灿芯半导体

打造国产先进工艺的一站式IP与SoC设计服务平台

饶青

2022年8月

Brite semiconductor

CONTENTS

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Brite Overview

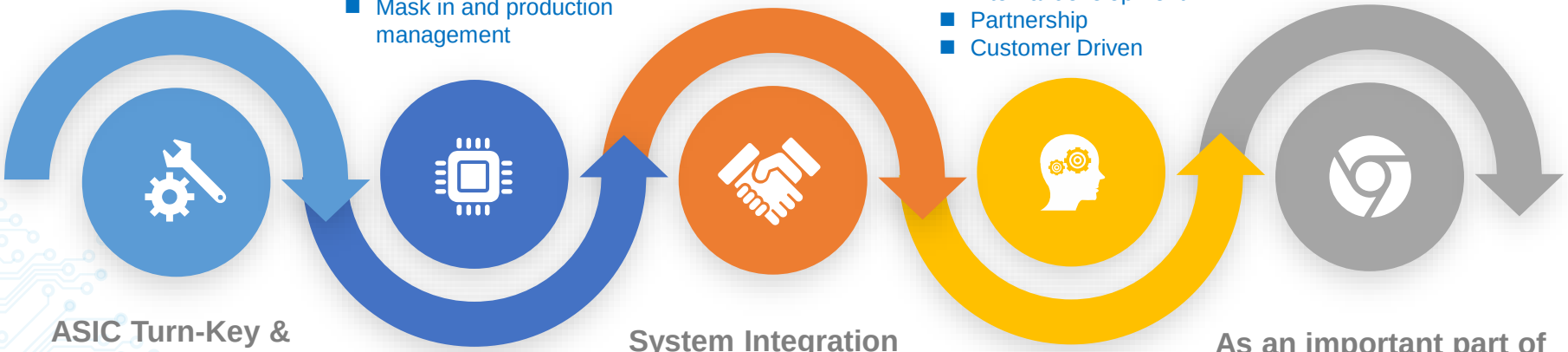
Brite's Service Offerings

Tape out & Manufacturing Services

- GDS in
- Mask in and production management

IP Procurement & Customization Services

- Internal development
- Partnership
- Customer Driven



ASIC Turn-Key & SoC Services

- Spec/RTL/Netlist to Silicon, complete hardware service
- Porting/Shrinking from an existing product to a derivative product, from FAB to fab

System Integration Services

- ARM CPU based
- RISC-V CPU based
- CEVA/Cadence DSP Based
- Synopsys CPU based
- Analog/ Mix-Signal

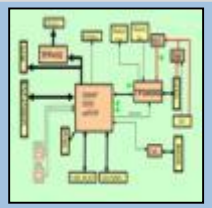
As an important part of SMIC eco-system

- Platform/IP development
- Design porting
- PDK QA & IP QA

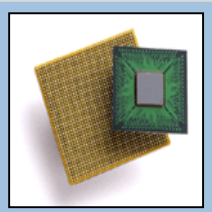
Total Solution: OEM+ODM

Customers

Product Specification

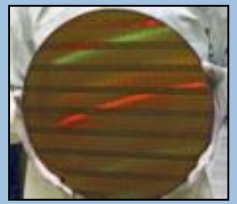


Architecture & RTL Design

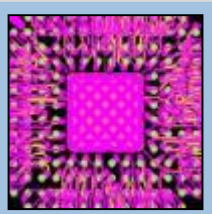


IP Selection & Integration

IC Physical Design



Wafer Fabrication

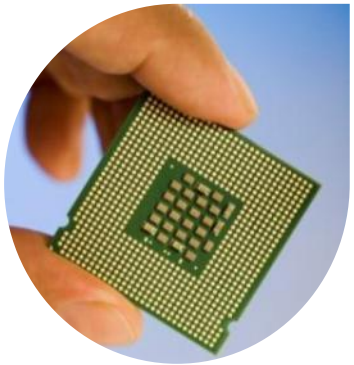


Package and Assembly

Test & Prod Engineering

Prod & Logistics

SDK Development



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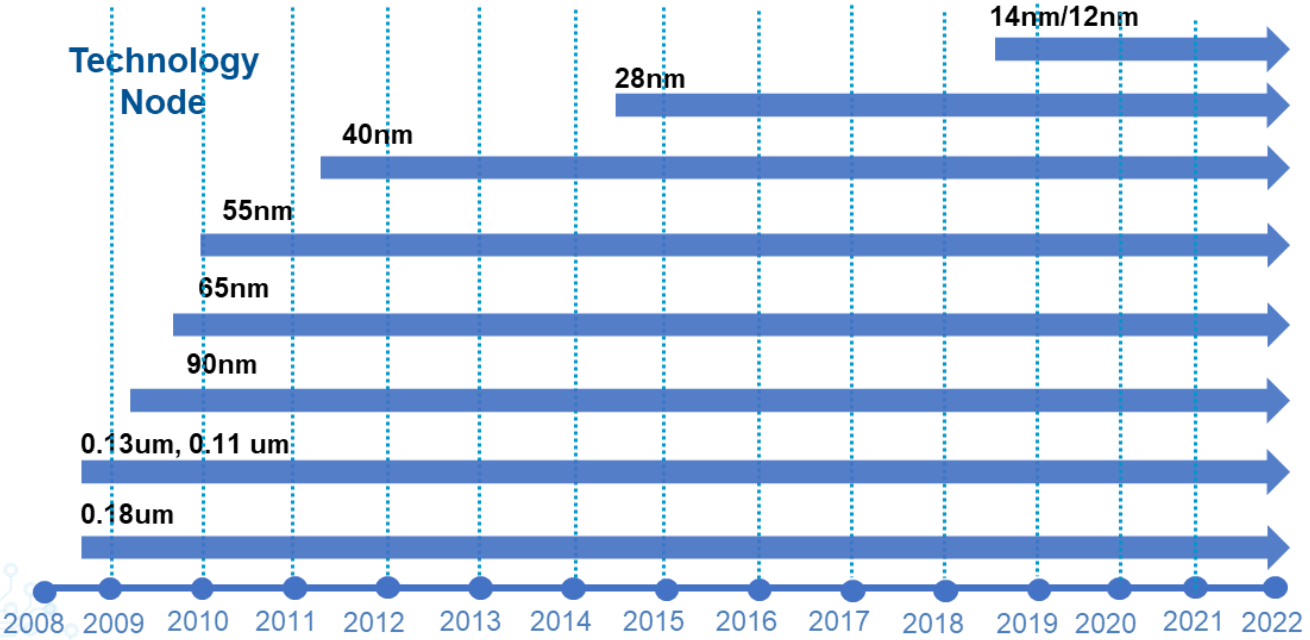
Platform and Services

Technology Roadmap



Technology Roadmap

Rich IP Availability

Std Cell/ Memory/IO	**Cell Library** 0.35um-12nm	**Memory Complier** 0.25um-12nm	**Std. IO** 0.35um-12nm	**SDIO** 0.11um-12nm		
Fundamental IP	**Regulator** 0.18um-12nm	**DC/DC** 0.18um-12nm	**Cap-less LDO** 0.18um-12nm	**Power On Reset** 0.18um-12nm	**Crystal OSC** 0.18um-12nm	
	Frac./SS/PLL 0.18um-12nm	**Comparator** 55nm-12nm	**Ring OSC** 55nm-12nm	**DLL** 0.13um-12nm	**Temp.Sensor** 0.18um-12nm	
ADC/DAC	**Sigma Delta ADC** 0.35um-40nm	**SAR ADC** 0.35um-14nm	**Pipeline ADC** 0.13um-40nm	**Audio/Video DAC** 0.18um-55nm	**Audio DAC/Codec** 0.18um-55nm	
HS Interface	**USB3.0/OTG** 0.13um-12nm	**USB2.0/OTG** 0.13um-12nm	**LPDDR1/2/3/4** 0.13um-12nm	**DDR2/3/4/5** 0.13um-12nm	**PCIe Gen 1/2/3/4/5** 65nm-12nm	**LVDS** 0.18um-12nm
	MIPI DPHY 0.13um-12nm	**HDMI2.0** 0.18um-12nm	**Display Port** 40nm-12nm	**SATA II/III** 0.65um-12nm	**Ethernet** 55nm-12nm	**SerDes (up to 32G)** 40nm-12nm
CPU Solution	**ARM Cortex A53/A55** 14SF+, 1.5GHz	**ARM Cortex A7** 40nm 1.1GHz	**ARM Cortex A9** 40nm 1.3GHz	**ARM Cortex M0/M0+** 0.13um EF	**CEVA TL421** 55nm	
	CEVA XM4 Quad Core 40nm-12nm	**CEVA DSP Core** MM3101,X1643,TL420,etc.	**AXI/AHB/APB/Arbiter/Bridge** 0.18um-12nm		**Digital Peripherals** 0.18um-12nm	

Brite Owned IP & Platform Solution

Advanced and Comprehensive
"YOU" IP Portfolio and Silicon Platform Solution

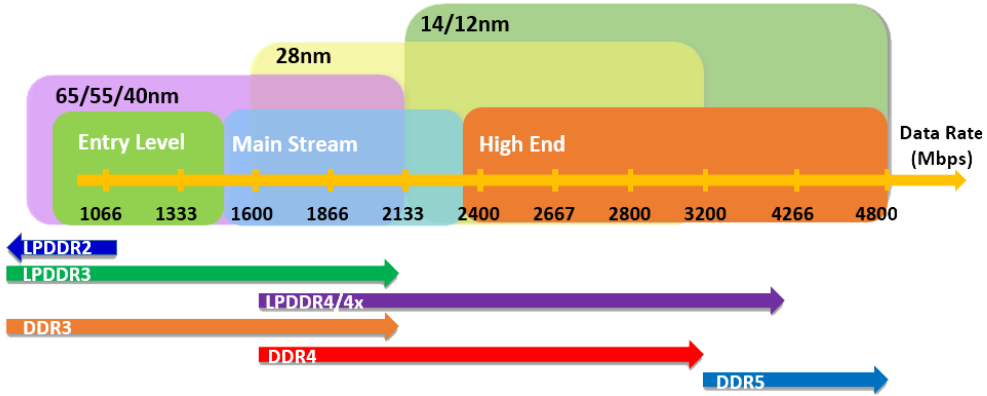
Brite YouIP & YouSiP

- **YouIP includes:**
  - YouDDR
  - YouSerdes
  - YouUSB
  - YouMIPI
  - YouPCIe
  - YouONFI
  - YouIO
  - YouRF
  - YouAnalog
  - YouSecure
  - YouCrypto
  - YouTCAM
  - YouADC
- **YouSiP (silicon platform) includes:**
  - YouSiP-IoM
  - YouSiP-Audio
  - YouSiP-Vision
  - YouSiP-IoT
  - YouSiP-AP
- **Each platform is silicon-proven and even product application proven**

Brite provides a complete DDR subsystem including not only controller, PHY and IO, also corresponding tuning and configuration software.

YouDDR is developed on 130nm to 12nm process respectively and support LPDDR2, DDR3, LPDDR3, DDR4 and LPDDR4/4x and DDR5 combo PHY with the data rate from 667Mbps to 4800Mbps.

With patented dynamic self-calibrating logic (DSCL) and dynamic adaptive bit calibration (DABC) technology, YouDDR can automatically compensate chip/package/board/memory PVT variation and bit-bit skew.



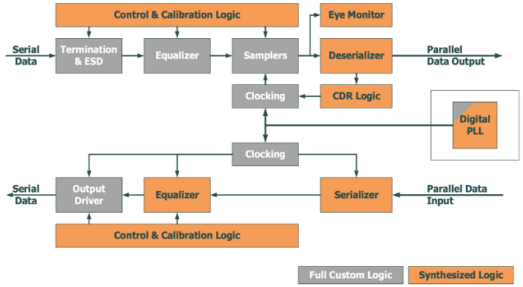
YouDDR Solution

YouSerdes provides 2.5Gbps-32Gbps multi-rate SERDES IP which is designed for smooth integration of multiple SERDES lanes offering best in class performance, area and power.

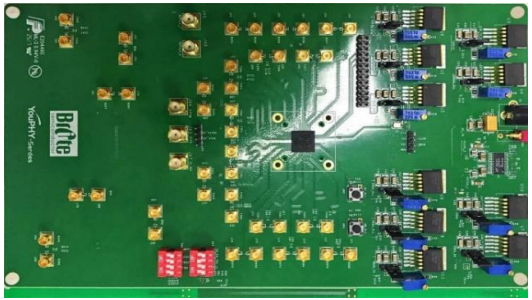
The programmable PHY supports major standards such as PCIe Gen 5.0/4.0/3.0/2.0/1.0, USB 3.1/3.0, XAUI, SATA Gen 3.0/2.0/1.0, CEI-11G-LR, 10GBase-KX4, JESD204B, SGMII/QSGMII, RAPID I/O, HSSTP (Trace Port), V-By-One, DisplayPort, HMC, based on advanced process as 12/14nm.

Power consumption@32Gbps ~8mW(single LANE+30mW CMU, -15dB insertion loss)
~10mW(single LANE+30m CMU, -30dB insertion loss)

Provider	Process	IP Category	Description	Status
Brite	14SF+/12SFe	Interface	32Gbps Combo PHY	Silicon Proven
	28HKC+	Interface	16Gbps Combo PHY	In-design



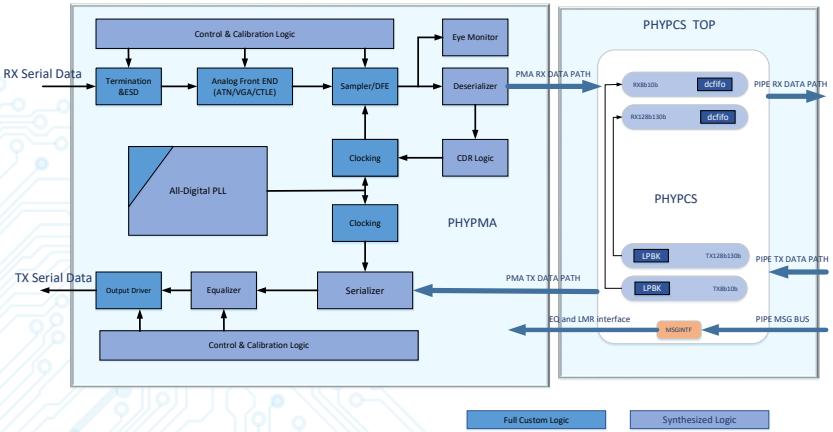
YouSerdes Subsystem



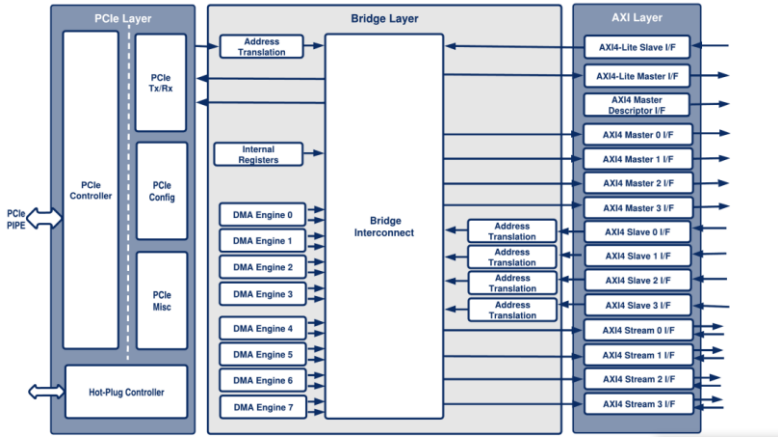
YouSerdes Demo Board

Brite 32Gbps PCIe PHY and controller solution provide high efficient interconnection that is optimized for PPA performance. The System can support short-reach or long-reach channels for plenty application scenarios. Besides the high performance of the PHY with its high line rate, low latency operation is a key feature of the PCIe PHY. The PHY supports data rate from 2.5Gbps to 32Gbps to cover PCIe Gen5.0/4.0/3.0/2.0/1.0. The common high-speed LC-PLL clock generation can supply clock up to 8+ lanes depending on jitter requirement, so that flexible macro configuration of e.g. 1x,2x,4x,8x are possible.

Brite PCIe controller to AXI architecture provides a high-performance, easy-to-use interconnect solution between PCI Express and the latest version of the AXI protocol. It inherits the leading architecture and features an AXI user interface with built-in DMA, compliant with the AMBA® AXI3 and AXI4 specifications.



Brite PCIE PHY Block Diagram

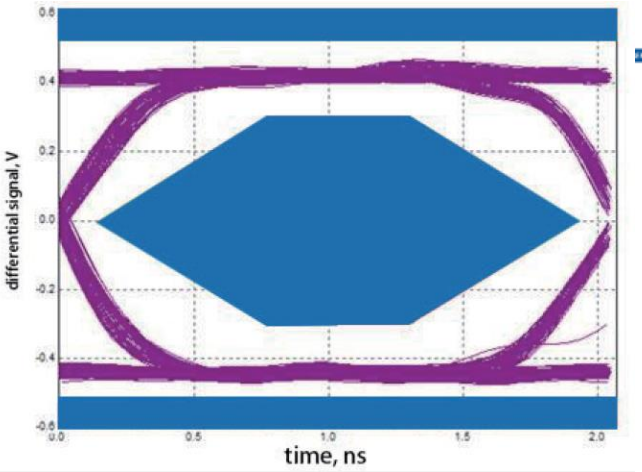


PCIE Controller to AXI Architecture

Brite provides USB2.0 OTG PHY which is a complete mixed-signal IP solution designed to implement OTG connectivity for a System-on-Chip (SoC) design.

The USB2.0 OTG PHY supports the USB2.0 480Mbps protocol and data rate, and is backward compatible with the USB 1.1 1.5Mbps and 12Mbps protocol and data rates.

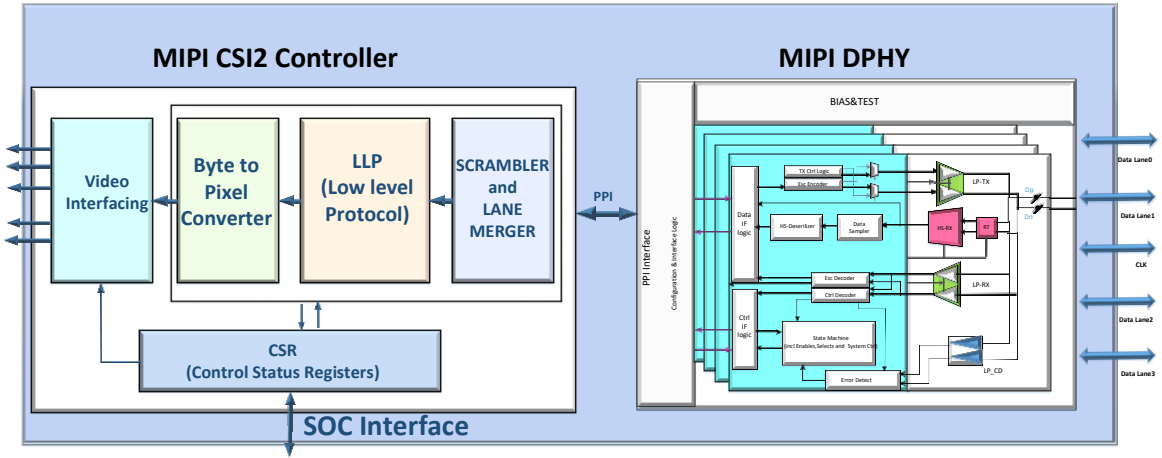
This solution can be adapted from 130nm to 12nm process. It has been verified by a number of end products, especially suitable for the internet of things (IoT) applications.



USB2.0 OTG PHY

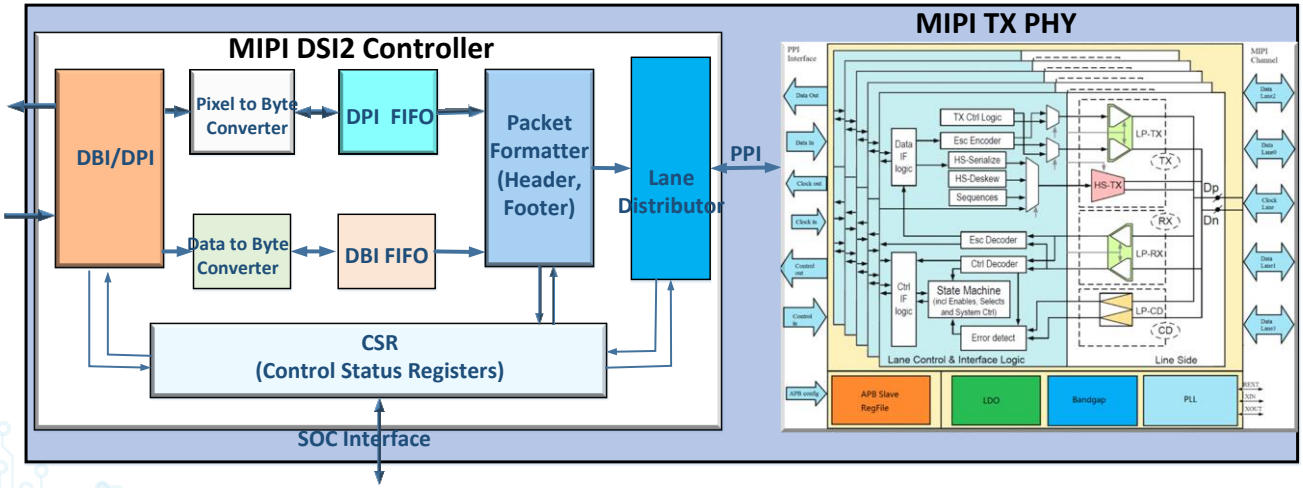
CSI2 Interface Solution

Brite provides a complete MIPI CSI2 interface, which receives the data from sensors in PHY layer, and then converts the byte data to pixel after lane data mergence. Data scramble is an optional feature to decrease the EMI effect. A standard PPI interface is implemented for the connection between MIPI PHY and CSI controller. Brite MIPI CSI interface solution supports image applications with varying pixel formats.



Brite MIPI CSI2 Interface Solution

Brite provides a complete MIPI DSI2 solution, which is compliant with MIPI DSI-2 specification. It supports 1 to 4 lane configuration and different data formats, which can adapt to diverse application scenarios. The DPHY can support crystal or SOC clock input as reference clock, and the data lane sequence can be freely swapped. The interface between controller and PHY is a standard PPI interface.



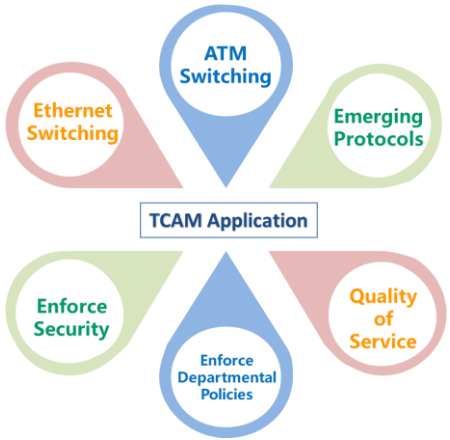
Brite MIPI DSI2 Interface Solution

YouTCAM Brite Ternary CAM Compiler

Key Features:

- **High yield**: In-house developed Bit Cell, matching logic design rule.
- **High reliability**: Logic bit cell design, avoid process violation.
- **Low power design**: Hierarchical search line and hierarchical matching line.
- **High performance**: Optimized PPA with full custom design.
- **High speed**: Working speed supports 1GHz.
- **High flexible design**: Memory compiler design.
- **High density**: Memory compiler supports maximum 1K x 160bits.

TCAM IP Basic Information	
Process	14nm SF+, 12nm SFe
Voltage range	0.72V~0.88V
Temperature	-40℃~125℃
Total bits	256~160kbits
Bit width	16~160 step=2
Word width	16~1024 step=8
Column Mux	1
Bank	1~8(base size)
Redundancy	1 column
Bit write/compare mask	Yes
Working speed	**1 GHz**



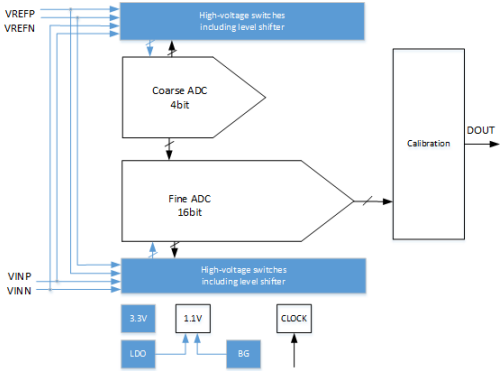
YouADC ADC Solution

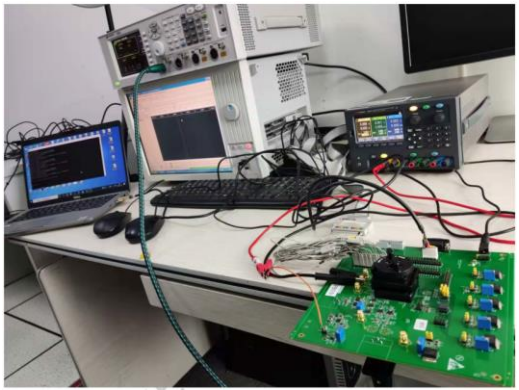
Brite Semiconductor offers customers a variety of ADC IP models, and the main architecture includes SAR and Pipeline, with the sampling accuracy of 12-16bits, and the conversion rate of 500K to 170Msps.

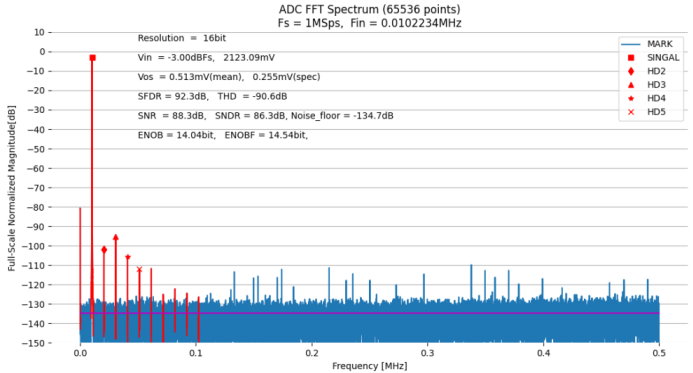
- 12 bits 100Msps SAR ADC on 14/28nm process;
- 12 bits 25Msps SAR ADC and Pipeline ADC above 100Msps on 40/55nm process;
- 16 bits 2/1Msps SAR ADC on 40/55nm process;

The above ADCs have been silicon proven and applied in customers' products, and the diversity can meet the differentiated application needs of different customers.

The current 16 bits high-precision ADC on 40/55nm process, provides an effective number of bits of 14 bits and the average effective number of bits more than 15 bits under the premise of ensuring the sampling rate of Msps, providing a variety of options for high precision industrial applications.





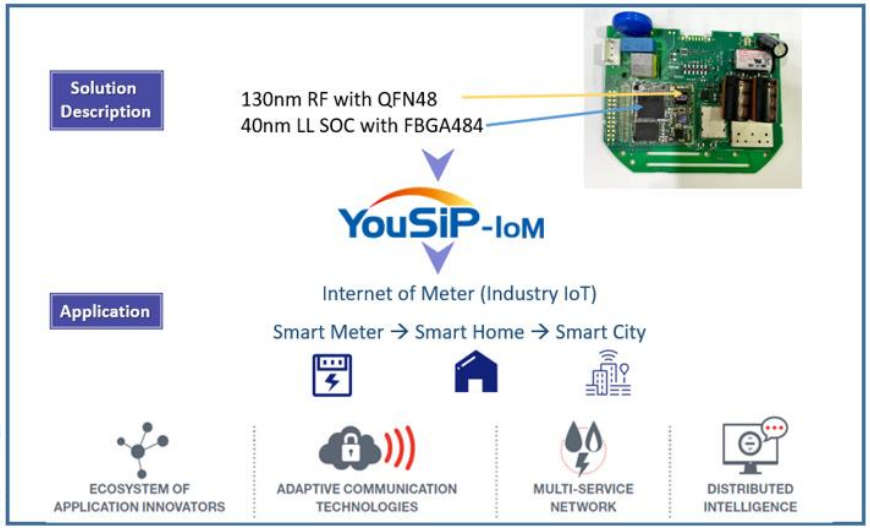


16bit SAR ADC Test Platform and Results

YouSiP-IoM(Internet of Meter) is an innovative interconnection SoC solution with 40nm LL process for smart meters.

YouSiP-IoM based on ARM Cortex A7 and Cadence Tensilica LX6 DSP architecture. Multiply transmission interface IPs are integrated to support industrial level wire and wireless connection as PLC, IEEE 802.15.4g and WiFi which can bring intelligent and connection to smart water, electricity and gas meters.

Abundant peripheral interface contains NAND Flash, LPDDR1/2, SD/MMC, USB 2.0 OTG, UART, SPI, I2C and RTC, which enable designer to extend sensing function and smart measuring technology and adapt product on various emerging applications and systems.

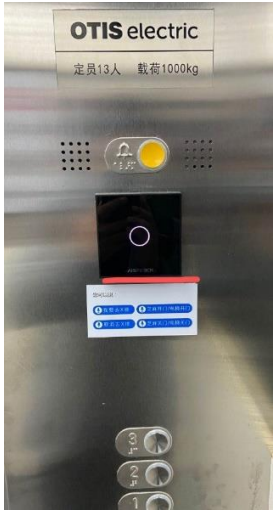


YouSiP-Audio is a SoC solution of voice recognition for AI application. The solution is based on 40nm process, with low power consumption and high performance, and is ready for mass production.

YouSiP-Audio solution can be adopted on various voice applications, mainly for smart home, smart devices, automotive, mobile and wearable devices, etc. The solution has the ability to quickly give voice interaction to various devices, can realize voice processing, voice recognition, voice broadcast and other functions, supports offline voice interaction and which can greatly improve user experience and product layout flexibility.

Key technologies: 40nm SoC low power design; efficient audio codec; voice wake-up; DSP custom instructions; configurable IO multiplexing function.

Customer Success Story
-Smart TV



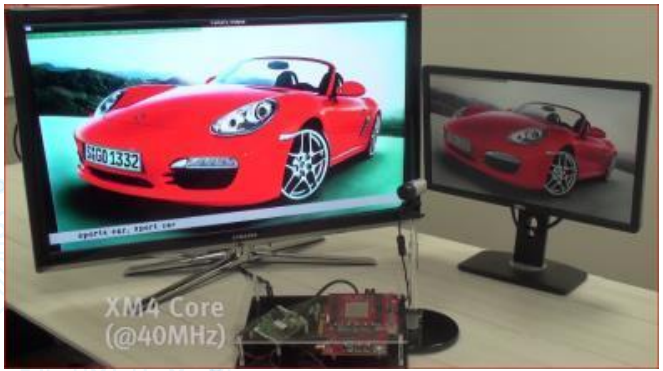
Customer Success Story
-Smart Elevator

YouSiP-Vision

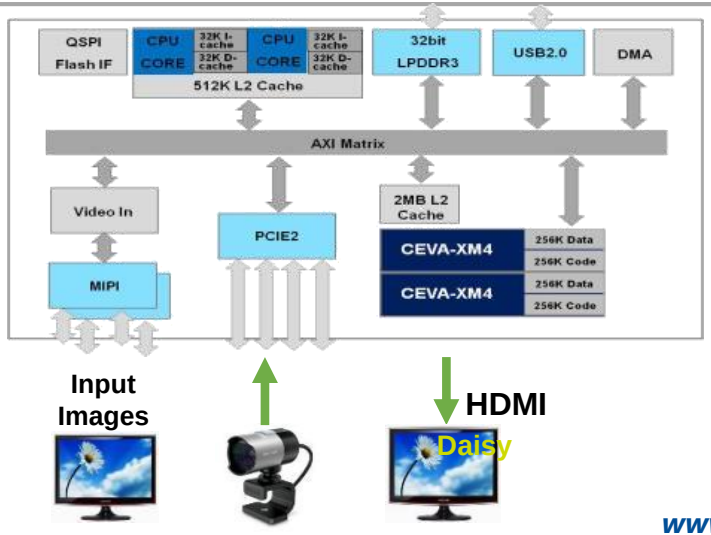
YouSiP-Vision is an image signal processer (ISP) platform integrated with CEVA XM4, and some high speed interface IPs as MIPI, PCIe, LPDDR3 and USB which is developed based on 14nm, 40nm process.

It can support 3D vision including real-time 3D depth map generation and point cloud processing for 3D scanning, computational photography algorithms including refocus, background replacement, zoom, super-resolution, image stabilization, HDR, noise reduction and improved low-light capabilities, visual perception including deep learning, object detection, recognition & tracking, context aware, augmented reality(AR) and others.

This platform targets any camera-enabled devices such as smartphones, tablets, ADAS and infotainment, robotics, security and surveillance, AR/VR and drones.



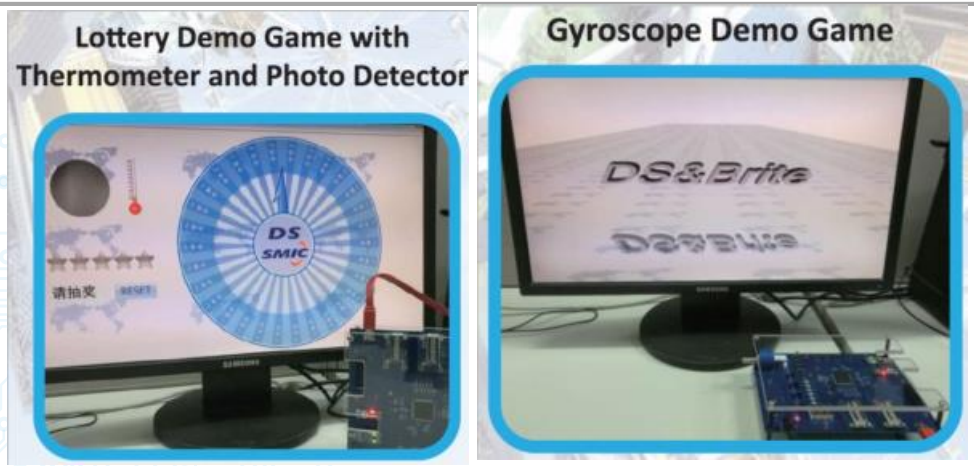
Real-Time CNN Object Recognition Demo



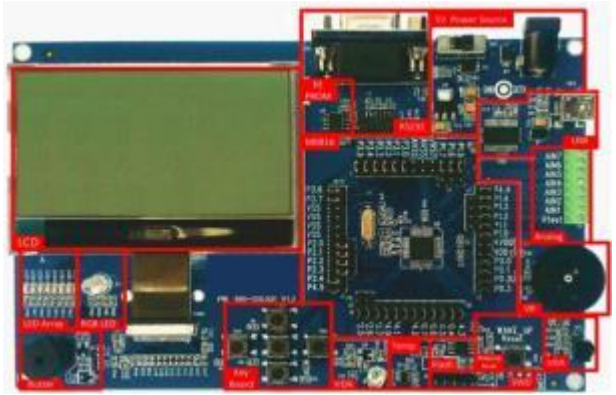
YouSiP-IoT (Internet of Thing) is a comprehensive platform solution designed for emerging application as IoT based on 55nm low leakage (LL) and 95nm ultra low power (ULP) process.

This solution integrates ARM Cortex Mx series MCU and CEVA TeakLite or MM series DSP, involves WiFi, Bluetooth/BLE interfaces, can connect to a series of different sensors.

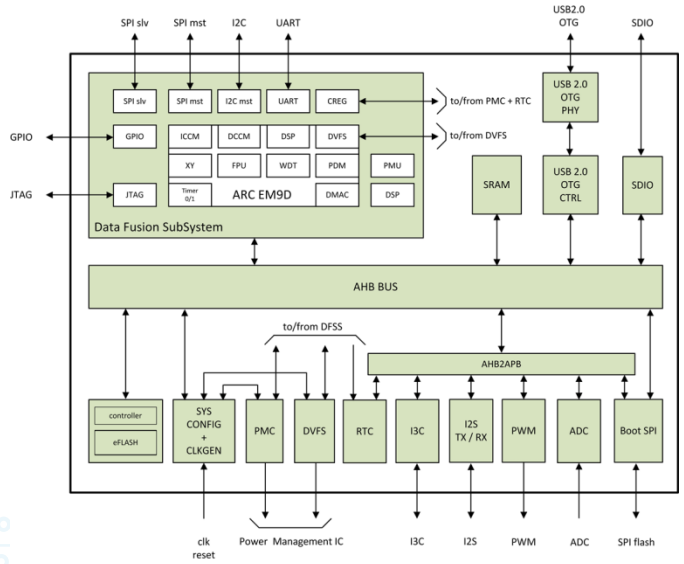
YouSiP-IoT platform can assist customer to reduce the processing delay time, enhance the data security, improve the data rate and reduce power consumption of their SoC design, which is adopted in battery power supply environment as smart home, IoT and wearable devices with excellent low power management.



YouSiP-IoT Application Demo System



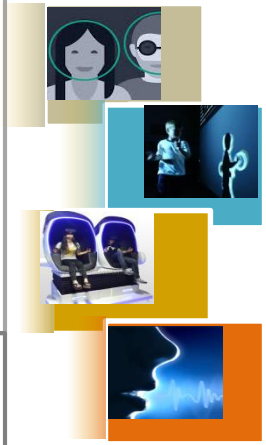
YouSiP-IoT Development Board



IoT platform

Process: 55nm LL / ULP
Key IP: DesignWare® ARC® Data Fusion Subsystem
Partners: SMIC, Synopsys, and Brite
Demos: Voice Detection, Face Detection & Gesture Recognition

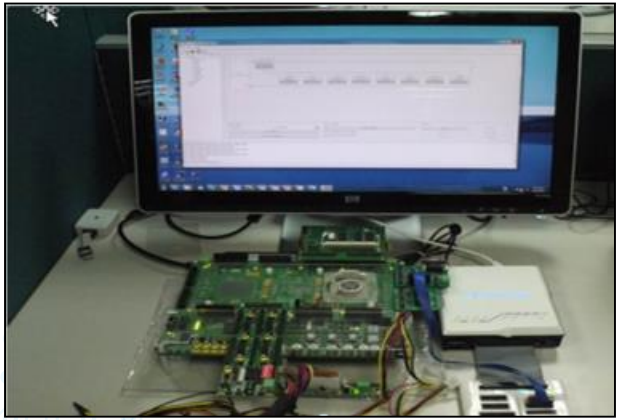
Application



- Low Power Face Detection
- Gesture Recognition
- 9D Motion
- Voice Detection Solutions

YouSiP-AP(Application Processor) provides an ARM Cortex-A series core architecture based SoC platform prototype which has been verified on 28nm and 40nm process.

Complete development tool including ISP/ICP tools, development boards, reference code and programmer and peripheral IPs can be offered to customer, enabling customer to achieve SoC product with shorter time to market and higher one time delivery rate, and assisting them win the emerging market opportunities in the field of industrial control, home appliance, security, toys, mobile devices, etc.



A9 FPGA Development Board

A9 Chip Testing Board

3

Success Stories

Success Stories

Process	Device	Application
14nm	Quad-core A53/Quad-core R8/Dual-core B20	5G
14nm	8-core A55/GPU/RISC-V	AI/Image Processor
40nm	Cortex-A7/Dual-core LX6	Smart Meter
40nm	HIFI DSP/Audio Codec	Audio AI
40nm	Cortex-A7/Base-band/10G serdes	Navigator
55nm LL	CEVA DSP/ 3 in SIP	Indoor Navigation
55nm EF	Cortex-M3 or M4/Flexray MCU	Industry MCU
55nm EF	RISC-V MCU	MCU
130nm	Digital	Safety System
130nm	Mix-Signal	Secure Solution
180nm	Mix-Signal	Led Driver

4

Summary

Summary

- ✓**Flexible business models and assist customer to shorter system to IC**
- ✓**Complete offerings in platform, IP, design, and manufacturing as a one-stop**
- ✓**High quality and on time delivery con**

THANK YOU!

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