

ACVS

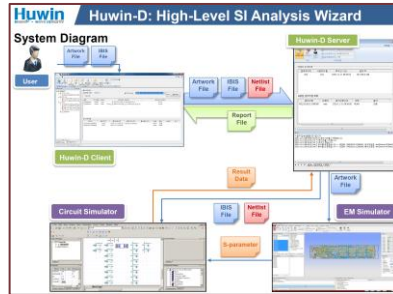
(Advanced Channel Verification System)

Next-Gen Signal Integrity Solutions for High-Speed Interfaces with Massive (1,000+ Ports) and Ultra-Broadband (100GB+ Size) S-Parameters.

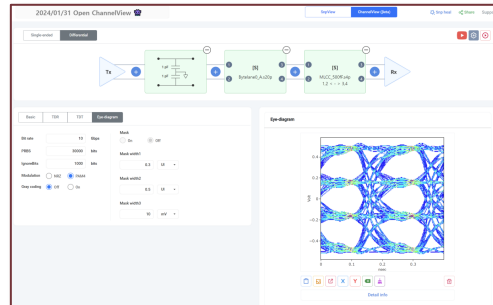


History

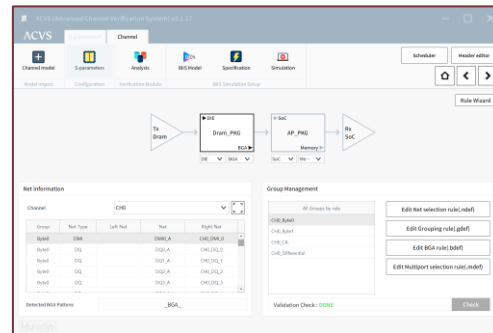
- Over 10 years, delivering the finest SI/PI solutions, ensuring trust and satisfaction among our clients.



Huwin-D



SnpView.Com



ACVS

2010

Huwin-D

- ✓ ANSYS simulation & reporting automation

GSI

Huwin-GSI

- ✓ Giga SerDes SI analysis
- ✓ EM automation
- ✓ Custom SI/PI analysis
- ✓ Report automation

SimNX

SimNX

- ✓ SI/PI analysis framework in freq./time domain



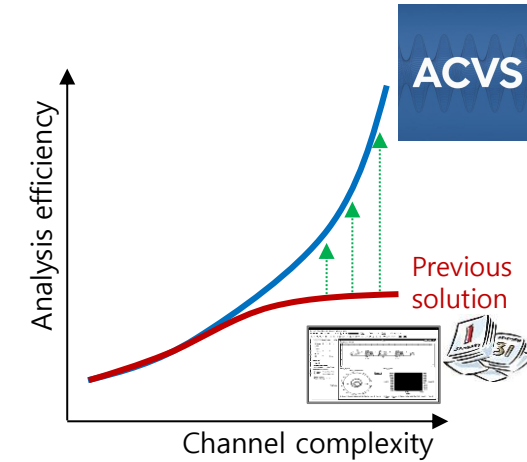
SnpView.com

- ✓ Web-based S-parameter analysis



ACVS

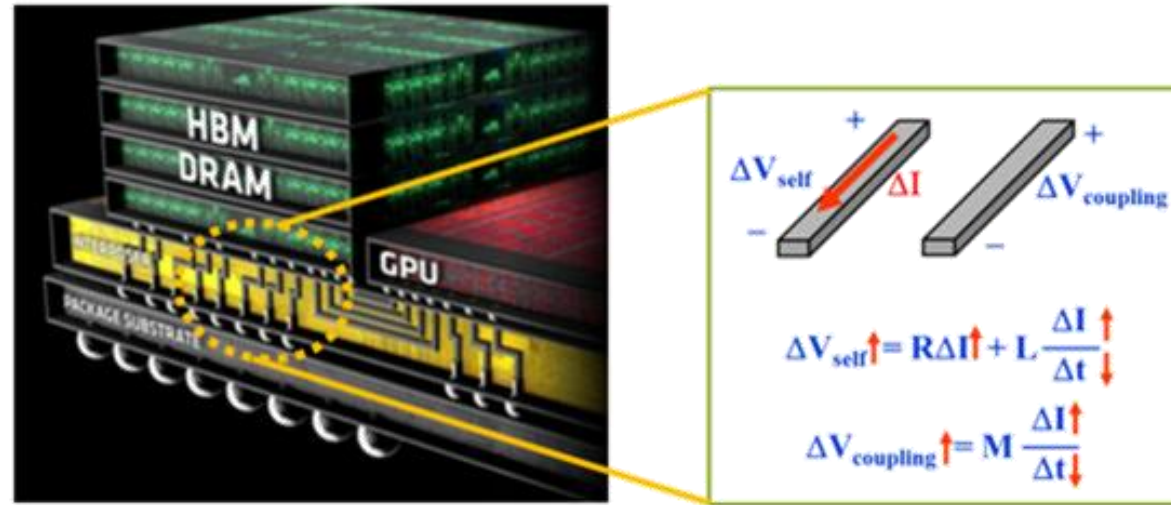
- ✓ Advanced Channel Verification System



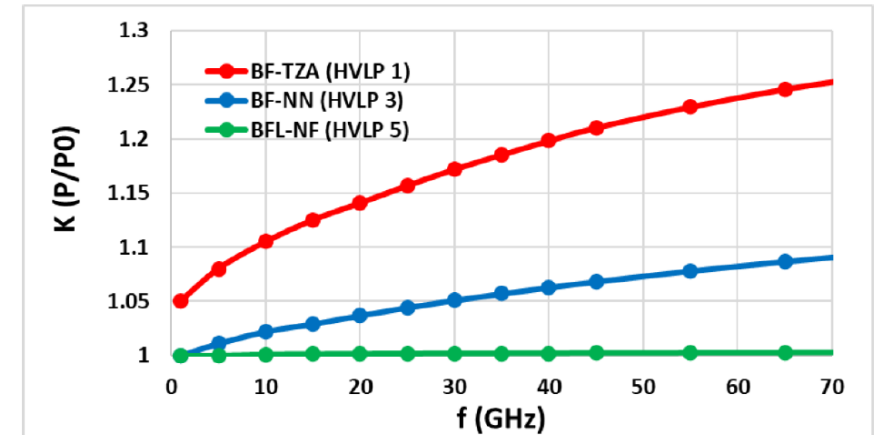
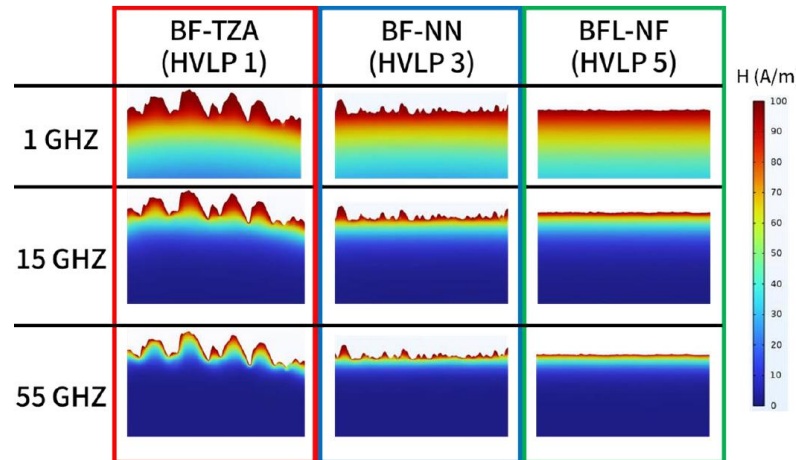
Tech. Issues : Advanced Package

Tech. Issues :

- S-parameters
- Impulse Response
- Jitter
- X-talks
- Return path
- RL, TDT
- IL
- Skin Effects
- PAM4
- Hardware Security
- Full Ch. Auto verification



• Smaller size & Narrower space



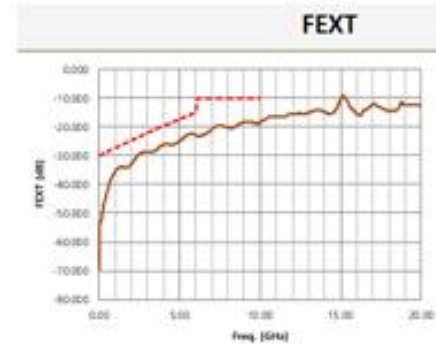
* Source : SLIDES_Track04_Finite element modelling of copper_Wittmann.pdf , DesignCon2023

Tech. Issues : Advanced Package

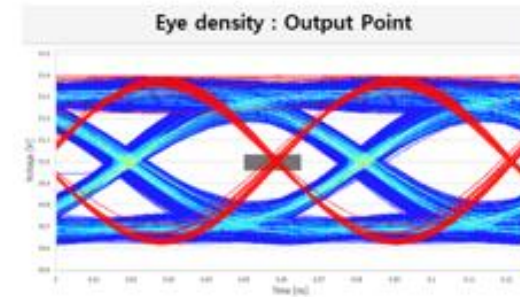
➤ Huwin ACVS Basic SI (FEXT) and Eye/BER report results correlation example for Jitter analysis

Tech. Issues :

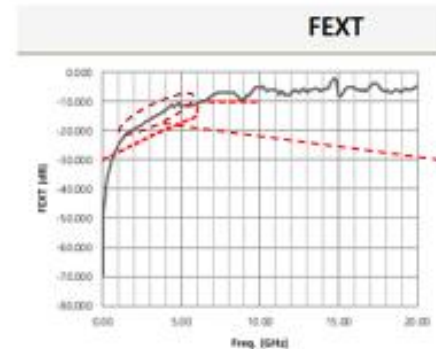
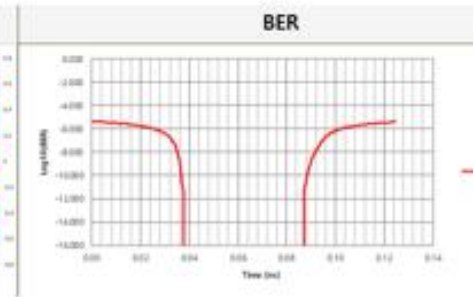
- S-parameters
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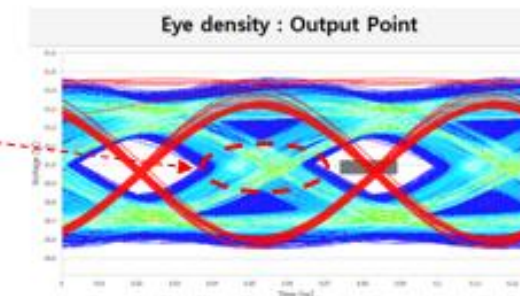
ACVS Basic report example of **Good ch.**
Satisfy the FEXT limit (far end cross-talk summation)



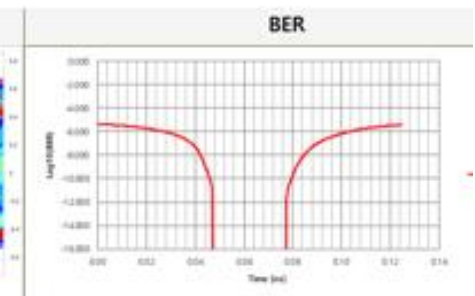
ACVS EYE/BER report example of **Good ch.**
With less Jitter noise



ACVS Basic report example of **Bad ch. Over**
the FEXT limit (far end cross-talk summation)



ACVS EYE/BER report example of **Bad ch.**
With more Jitter noise caused by FEXT

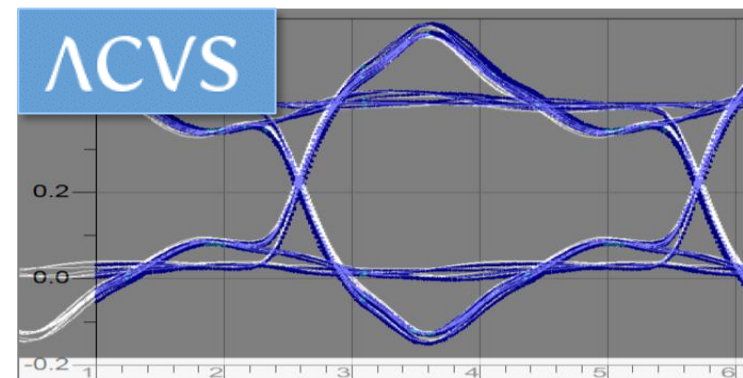
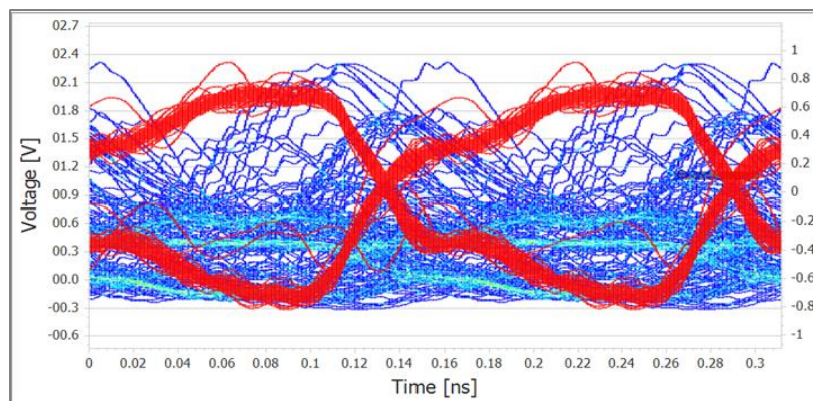
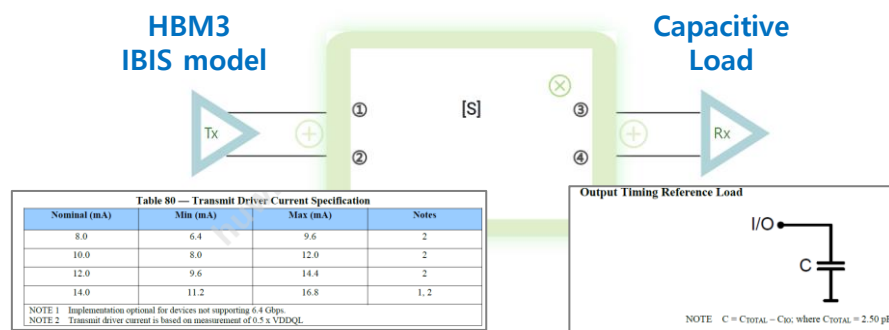


Tech. Issues : Advanced Package

Transient Solver for Advanced Package HBM Eye-diagram/BER analysis

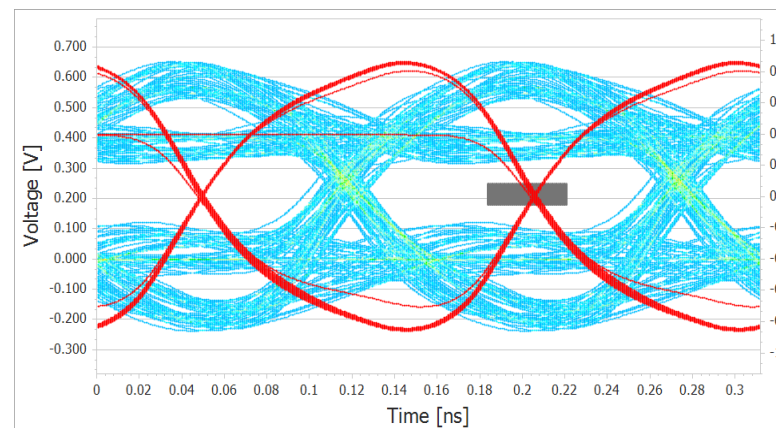
: ACVS Transient solver (SimNX) development for HBM

-> enhanced solver for the HBM channel and model



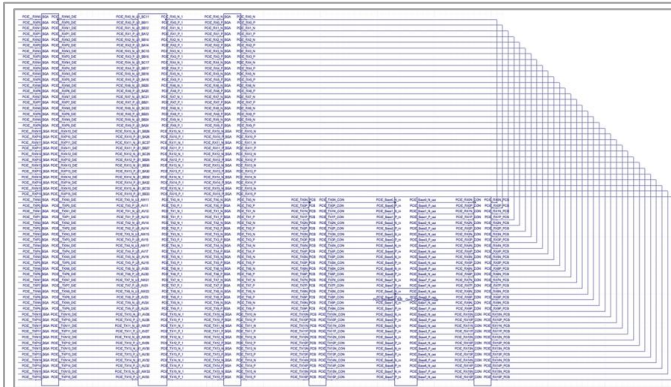
Improved ACVS Transient solver (SimNX) results

➤ Resolve the divergence problem

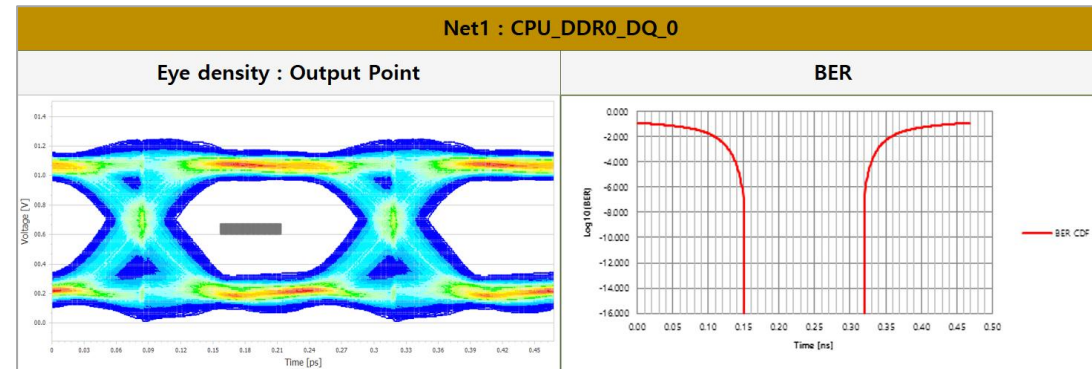
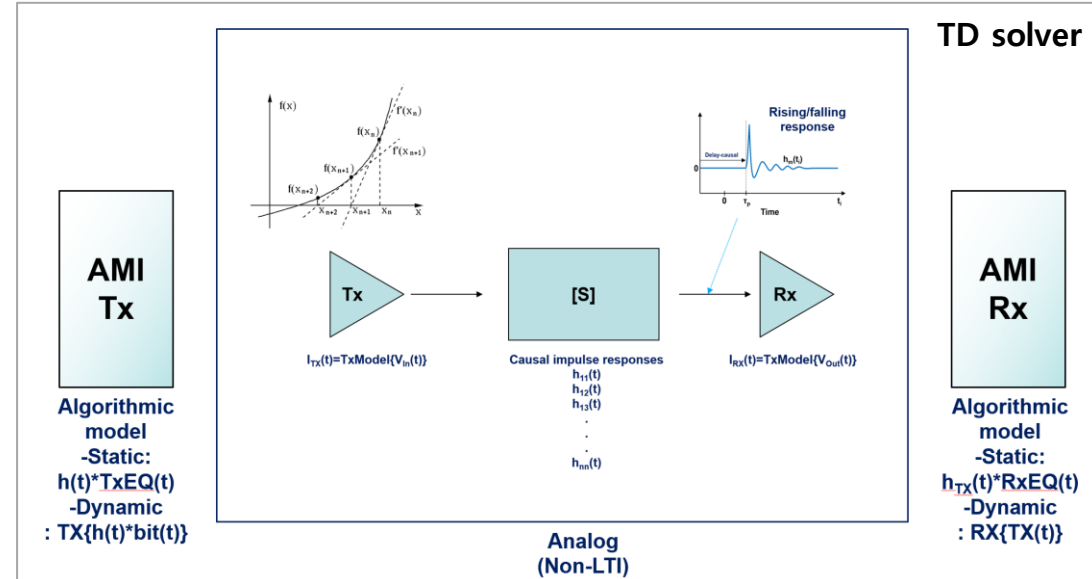
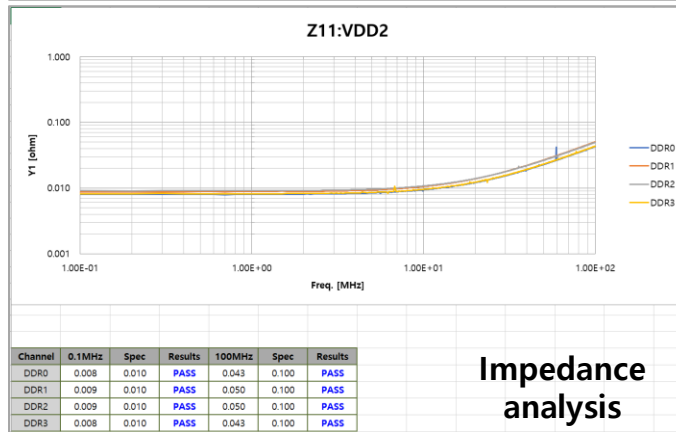


SI/PI analysis specialized solver framework

- Including frequency/time domain **circuit solvers** (SPICE like), **2D FEM**, and **post-processor**
- Goal: **Higher accuracy, efficiency and flexibility**



Efficient processing 
for large-size S-parameter matrix
: Connecting, combination, termination...
(enabling GDDR6, PCIe Gen5, etc.)



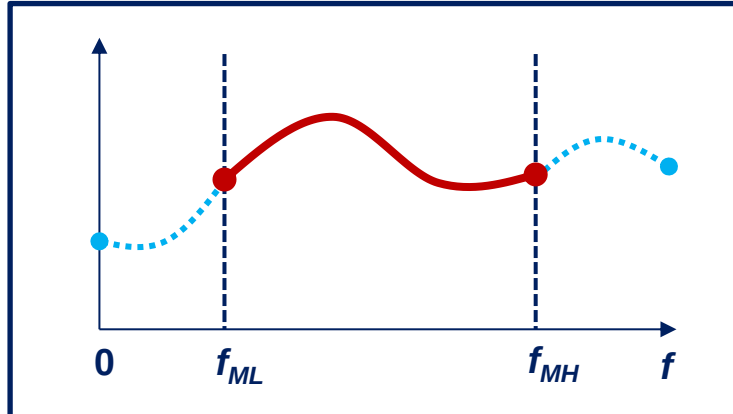
Eye-diagram, BER analysis

Extrapolation for extracting causal time response

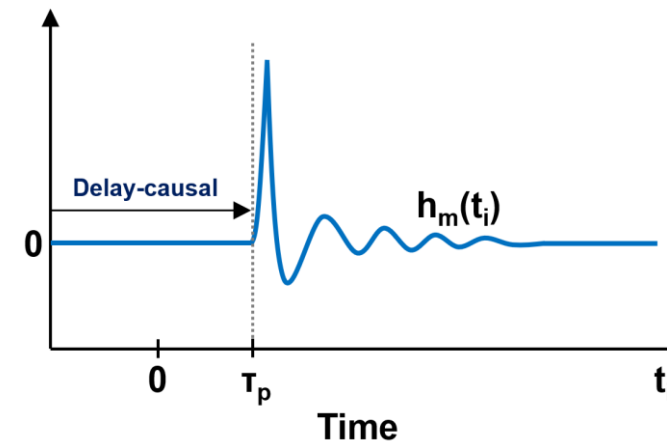
- Low/high frequency range extension
- Ensuring low frequency accuracy and causality of time response

	Direct IFFT, 1991	Vector fitting, 1999	Conventional extrapolation, 2008	SimNX extrapolation, 2018
Accuracy	Low (non-causal)	High (fine fitting)	High (step resolution)	High (LSE)
Causality	X	O	O	O
Low Freq. data	Required	Required	Required	Extrapolation
Propagation delay	Not required	Required	Required	Delay estimation
Efficiency of the method	High (IFFT only)	Mid (iterative fitting)	Low (iterative search)	High (non-iterative)
Applied solutions	-	Solution 2	Solution 1	Huwin ACVS, SnpView

Extrapolation of the band-limited S-parameter



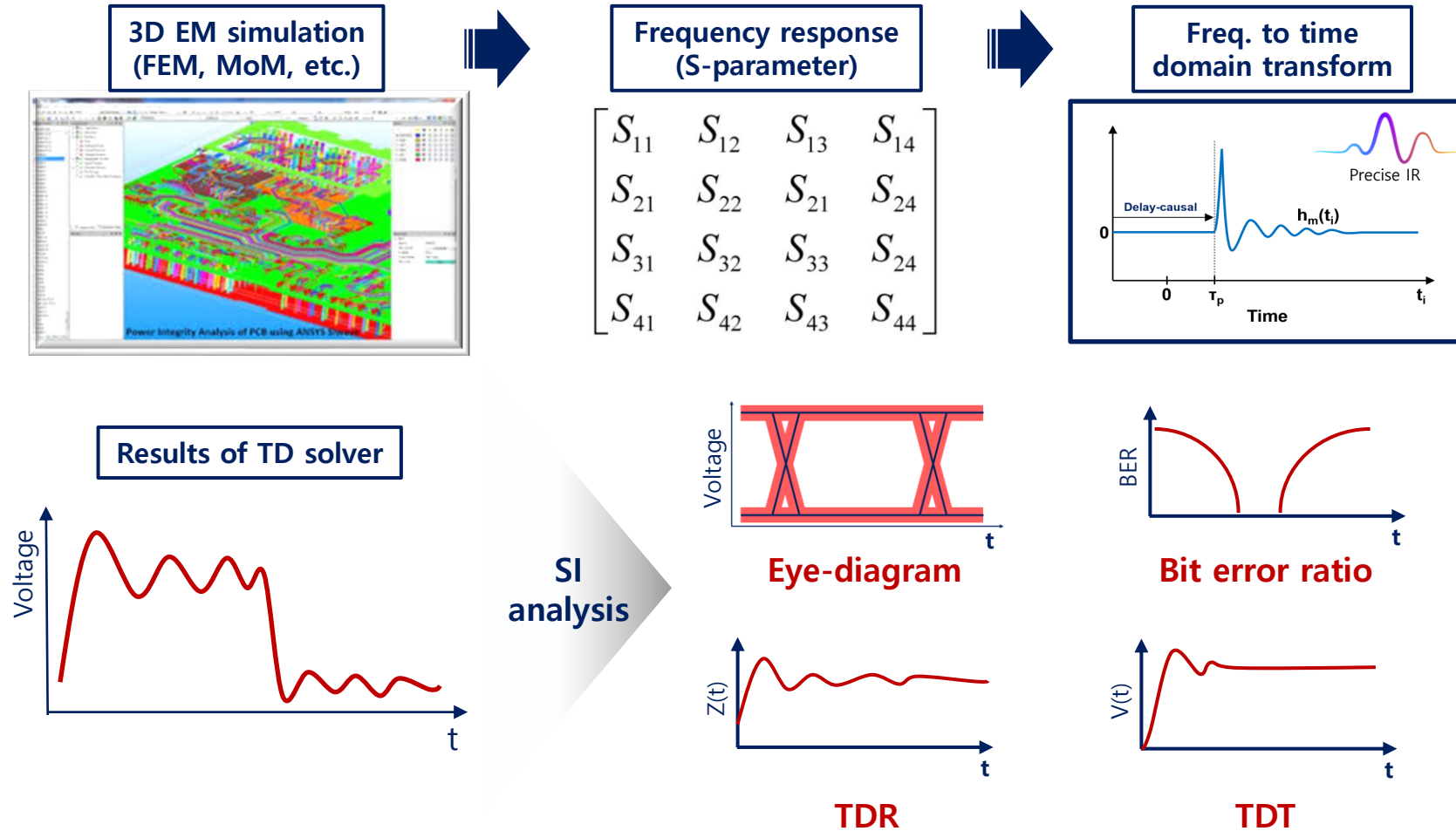
Causal time response



2. SimNX: Time domain Solver

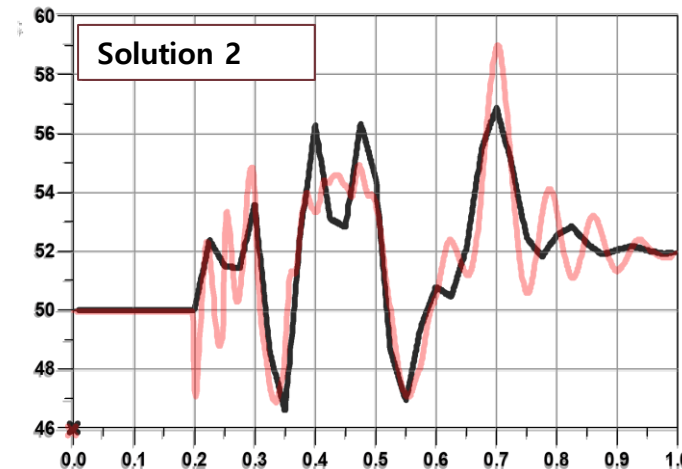
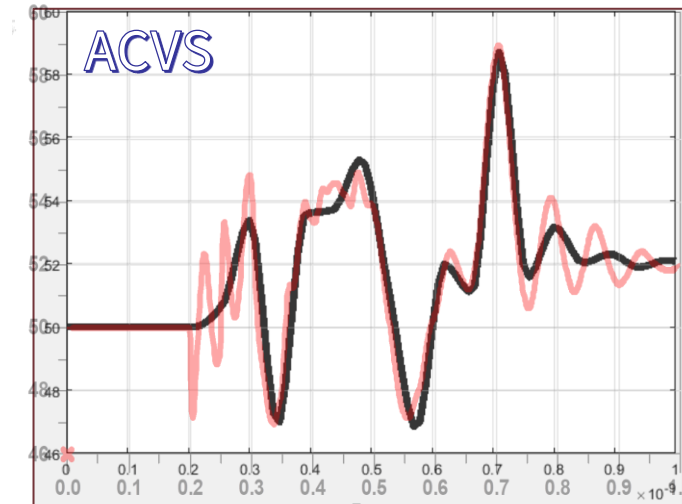
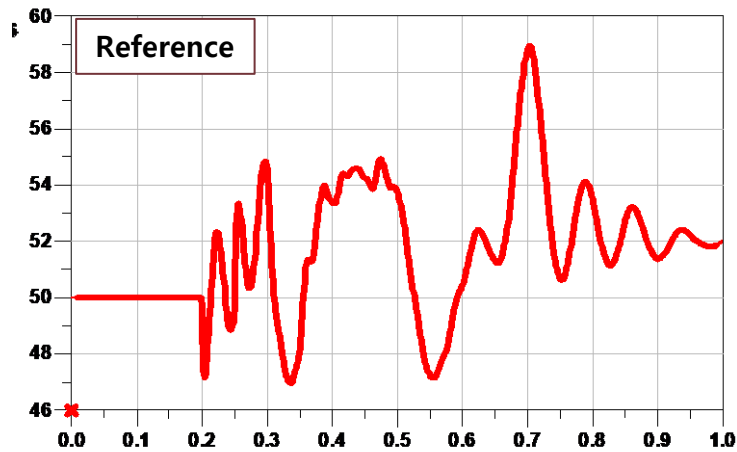
Improved accuracy, efficiency, and stability for signal integrity analysis

- Support: Full transient, channel Sim. with AMI model (single, diff.), TDR, TDT, etc.



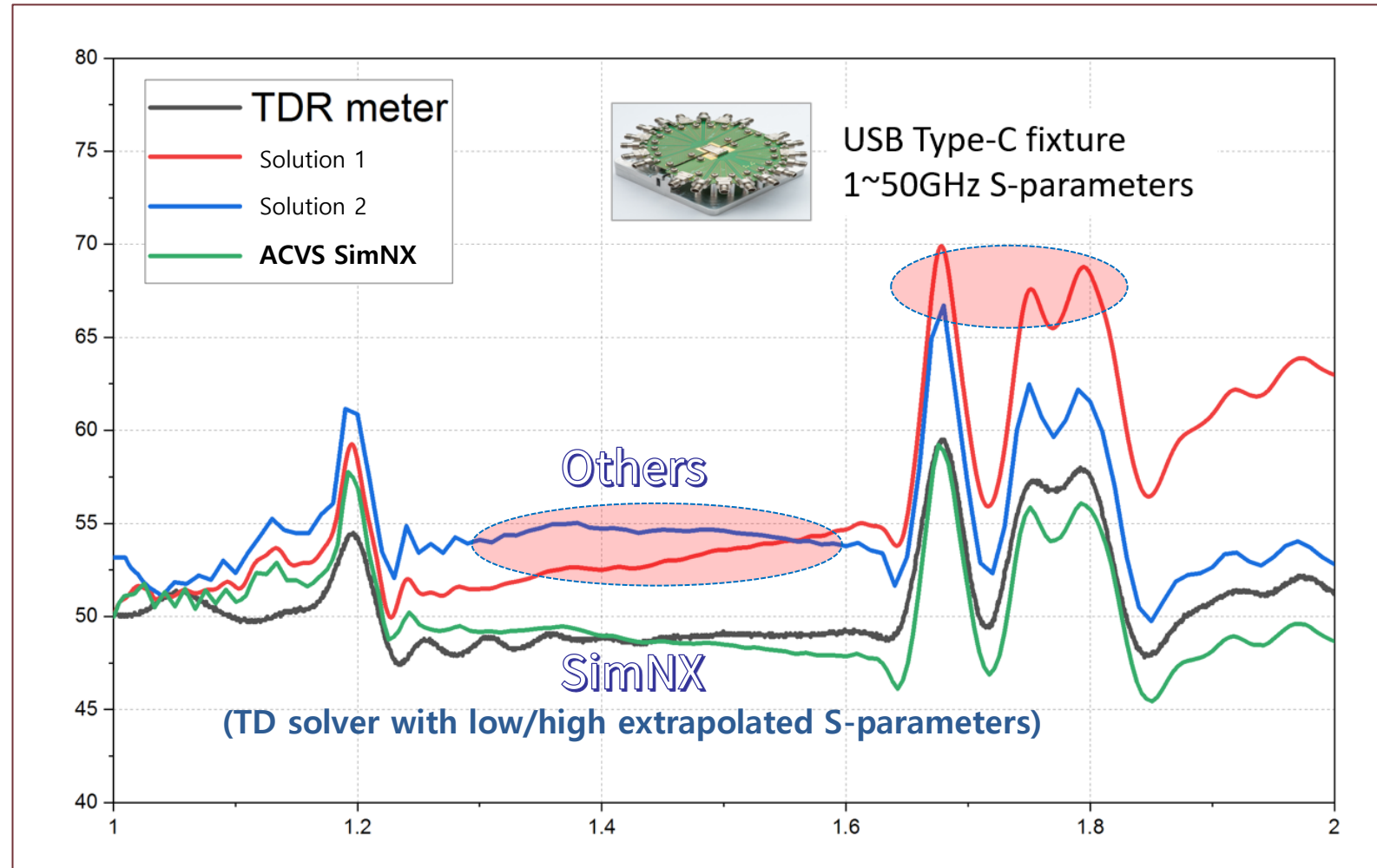
Case study: TDR

- Full band S-parameters (up to 500GHz) -> ACVS TD solver -> Reference results
- Truncated S-parameters (up to 10GHz) -> ACVS TD solver -> Results for the accuracy test



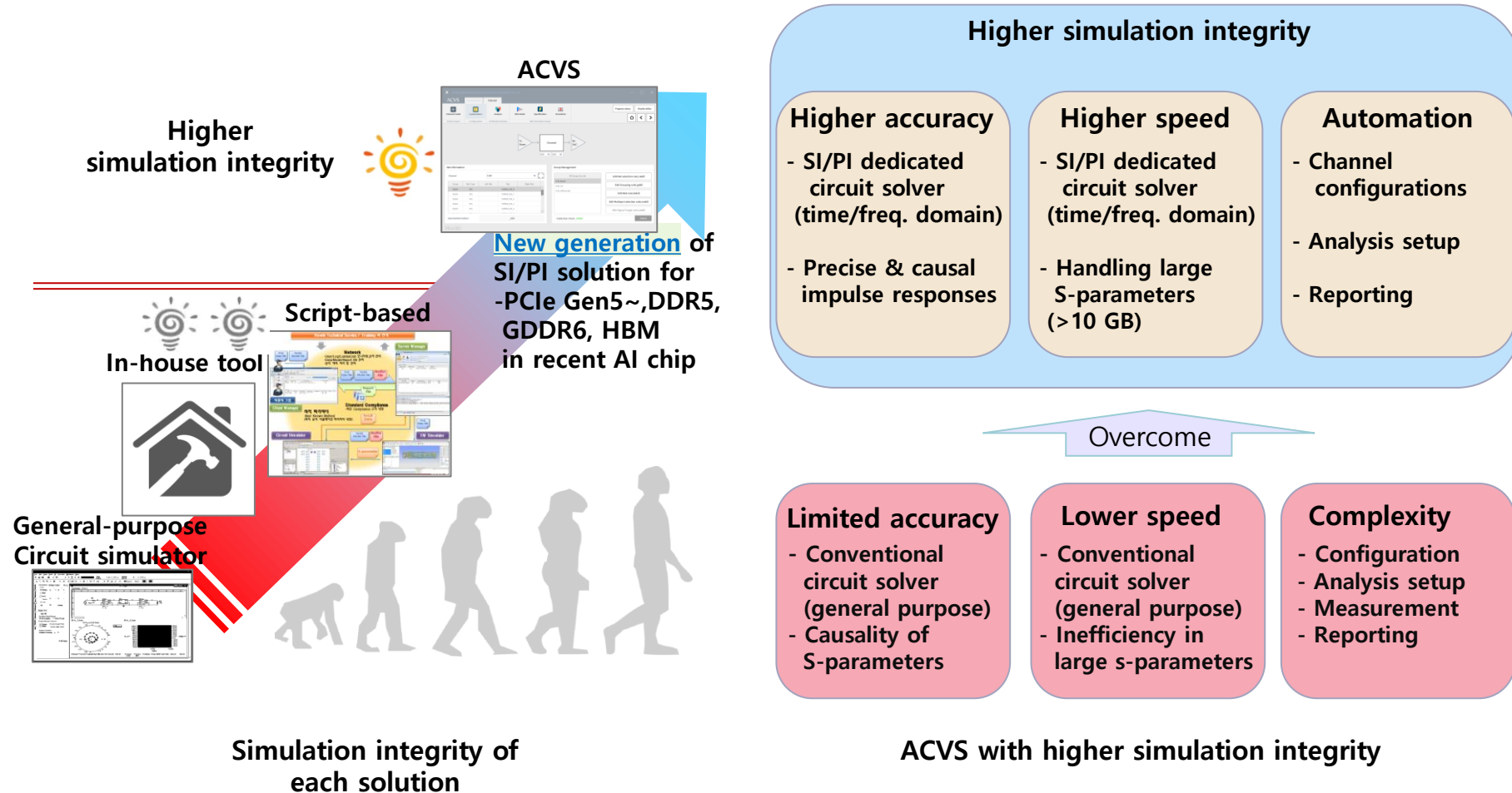
Case study: TDR

- TDR meter vs SimNX and other solutions with the truncated S-parameters
- Accuracy: TDR meter $\approx$ SimNX $\gg$ Other solutions



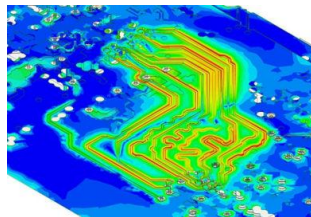
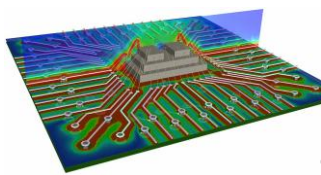
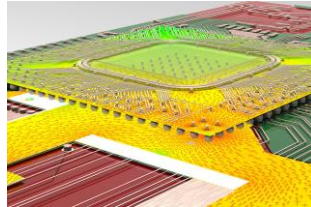
Key Requirements for recent channel systems (ex. HBM, UCIe, DDR, and PCIe)

- Enhanced accuracy and speed through fully automated simulations
- Time and cost reduction with improved accuracy and reliability in SI/PI analysis



High-Precision, High-Speed, and Reliable SI/PI Analysis

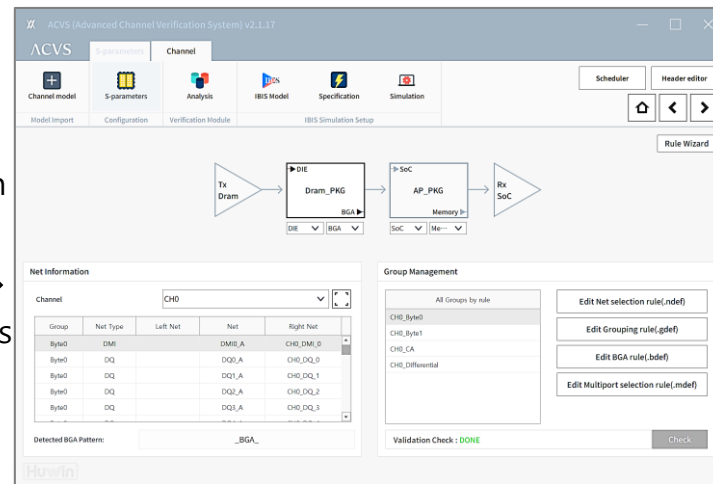
EM simulation



- ANSYS Siwave, HFSS, etc.

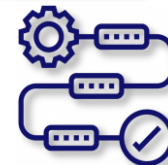
Automation
S-parameters

ACVS: Channel simulation/reporting

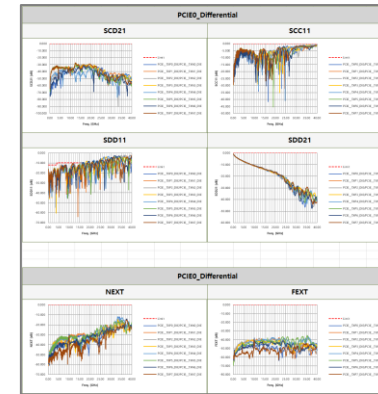


- Automation of system simulation with **SimNX®** engine.
- Reporting: charts and measurement.
- Applications: DDR4/5~, **HBM3+**, **PCIe**, **UCIe**, C-PHY, etc.

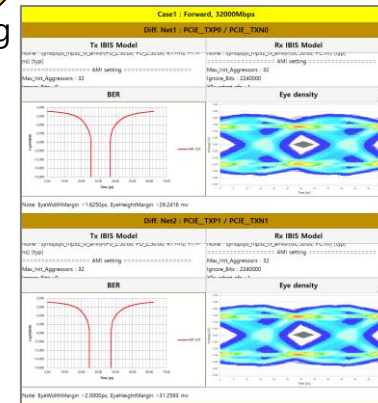
**S-parameters with 1000+ ports,
100GB+ file size**



Report



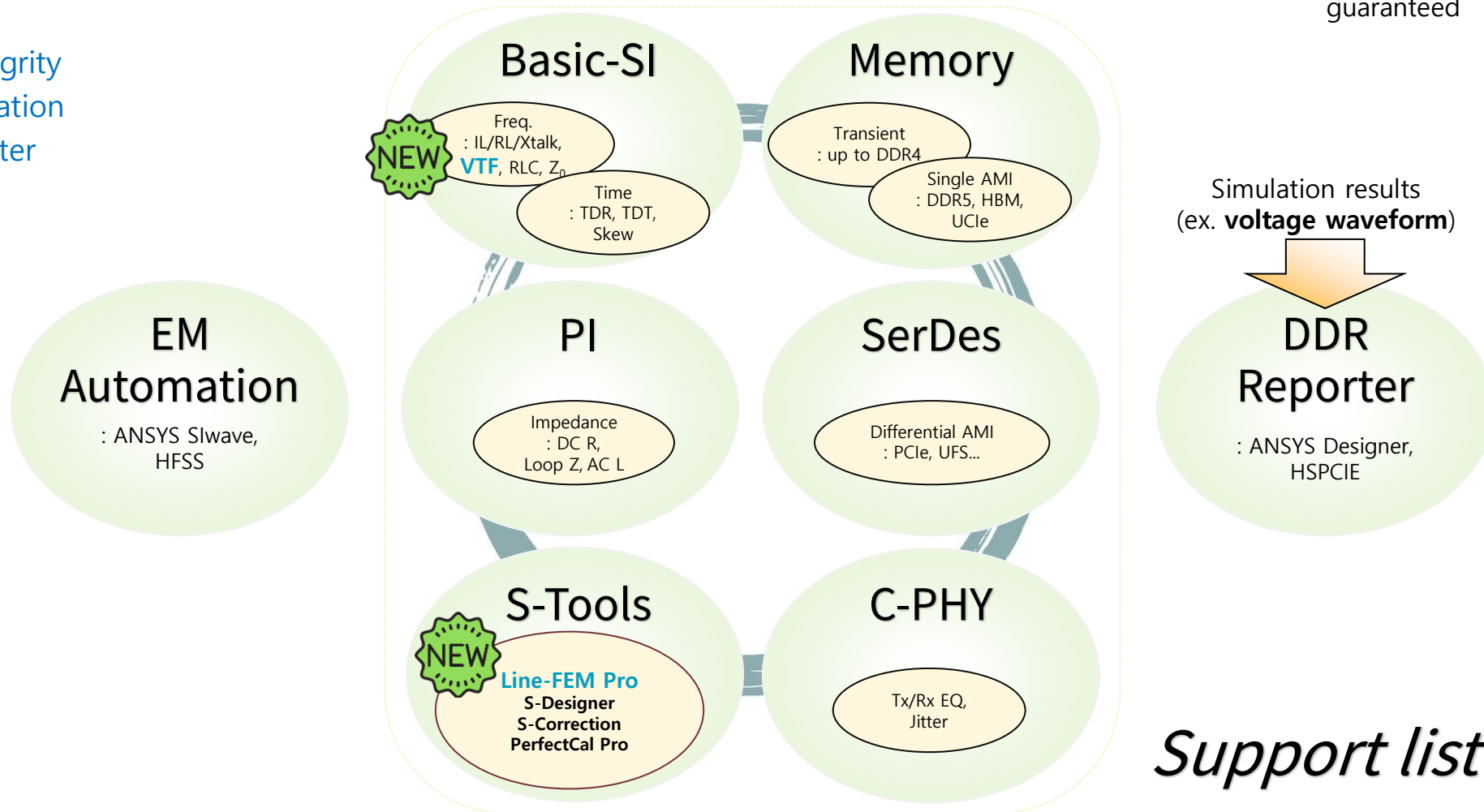
Reporting



- Customized report

Expanding **automation coverage** for recent applications

- **Basic-SI**: SI/PI essential analysis module in freq./time domain. Standard free
- **SerDes**: AMI channel sim. (ex. PCIe, UFS)
- **Memory**: Transient, AMI channel sim. (ex. (LP)DDR4/5~, HBM3, UCIe)
- **C-PHY**: Transient with Tx EQ, Rx CTLE, Jitter
- **S-Tools**
- Power integrity
- EM automation
- DDR reporter

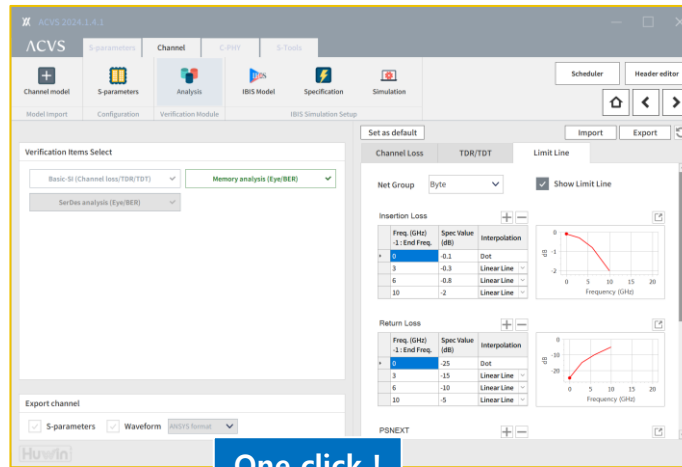


Basic-SI: Quick and easy verification for essential SI analysis

- 'One click' -> 'All essential SI charts'
- [Frequency domain] IL/RL/X-talk, Group delay, RLC extraction, Z_0 , VTF, etc.
- [Time domain] TDR, TDT, Skew etc.
- Exporting single S-parameter file of the combined channel.



Accuracy/Time
guaranteed

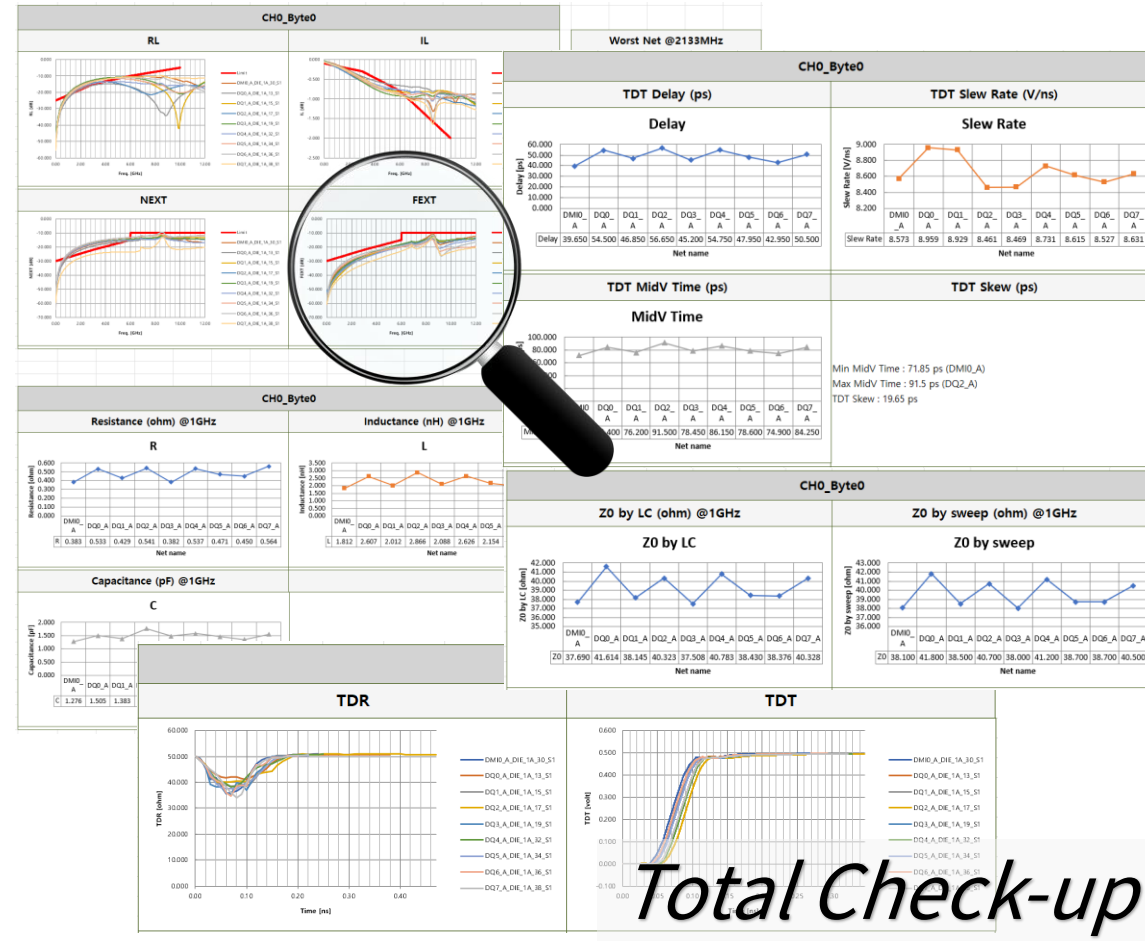


One click !

All essential SI charts!!

Channel.s#p

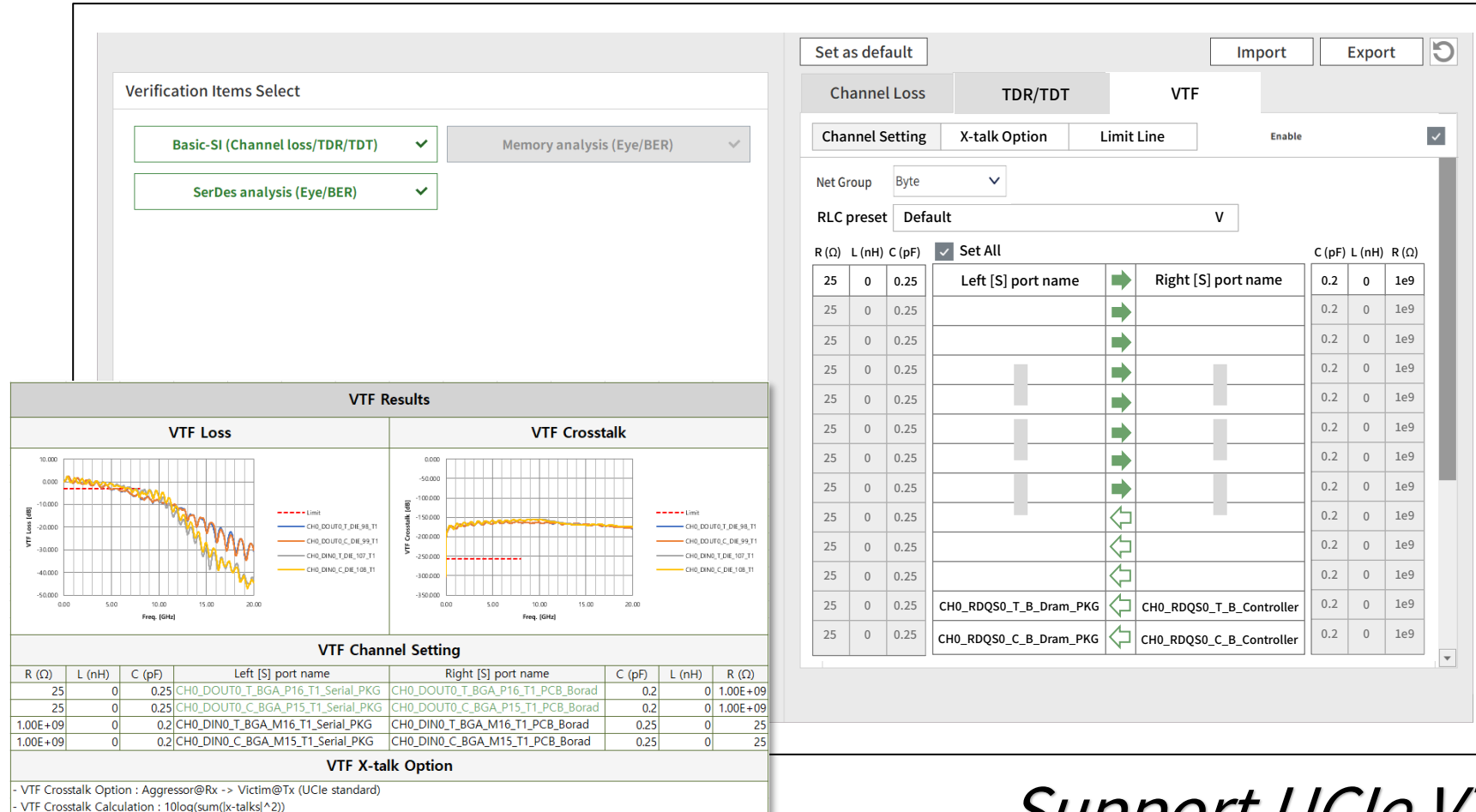
'Advanced channel connection method'
for preserving all frequency points
of each .s#p files



Total Check-up

Comprehensive environment for UCle VTF Analysis

- Bi-directional analysis configuration support
- UCle 2.0 standard Tx/Rx RLC and limit line settings
- Automated report generation feature



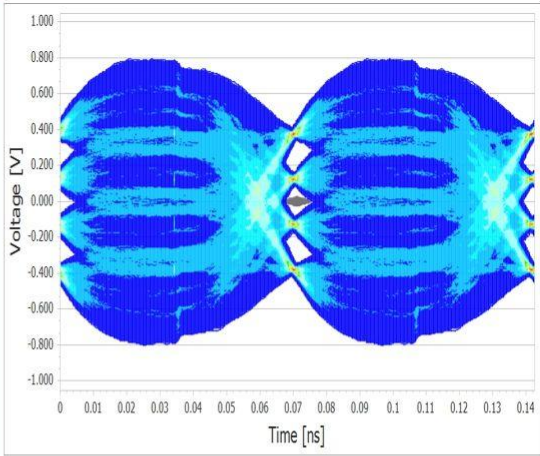
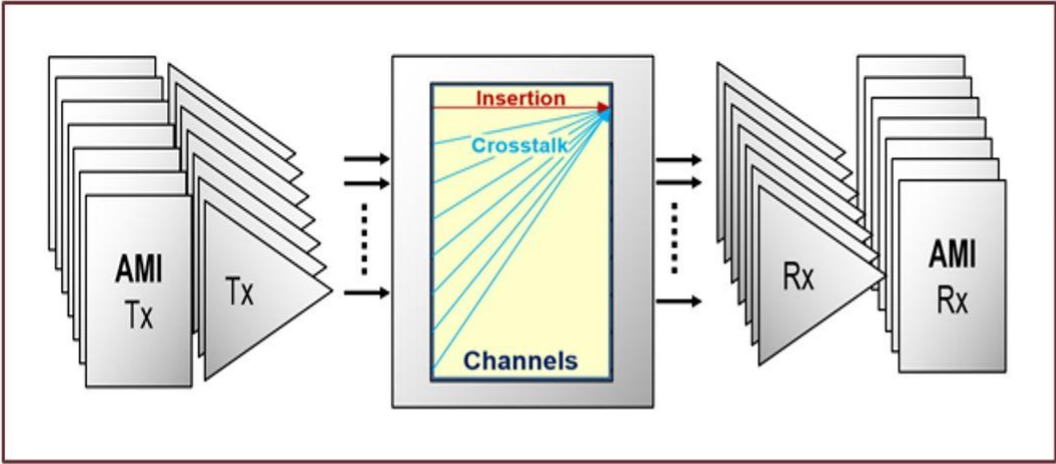
Support UCle VTF

- Supports all X-talk effects in SerDes AMI simulation
 - Fully automated in SerDes AMI simulation including all X-talks. + Basic-SI



FIRST & ONLY

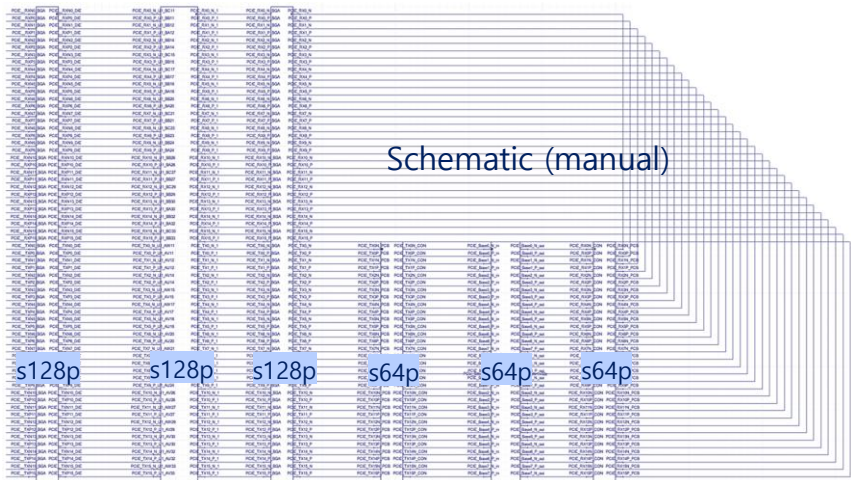
X-talk



SerDes AMI Analysis	Competitor 1 (circuit simulator)	Competitor 2 (circuit simulator)	Huwin ACVS (SI solution)
Single Pair with Cross-talk	Not Supported	Support	Support
Full Channel Pairs with Cross-talk	Not Supported	Not Supported	Support
Report Automation	Not Supported	Not Supported	Support

Support all

Case study: PCIe Gen5 (32 Gbps, IBIS-AMI, 16 diff. pairs, including all X-talks)



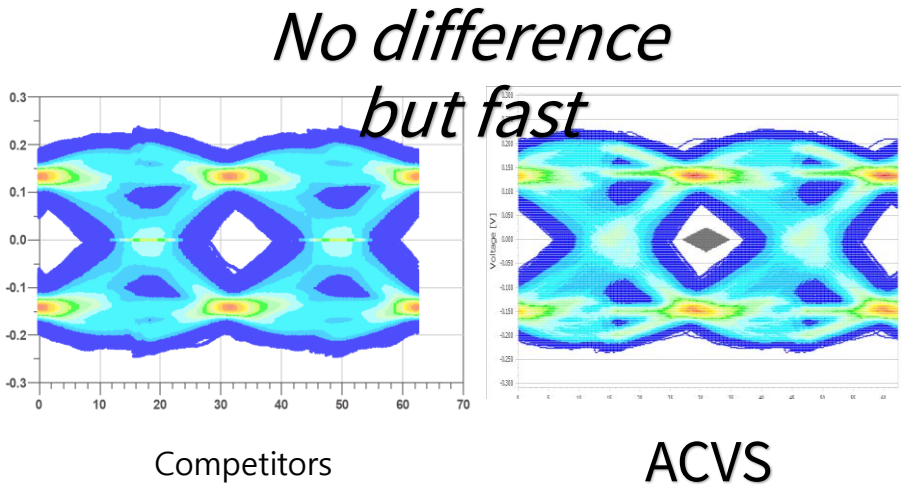
Schematic (manual)

Tx/Rx AMI models + Channel S-parameters
PRBS: total **2,270,000 bits**
(=ignore bits: 2,240,000+ input bits: 30000, PRBS15)

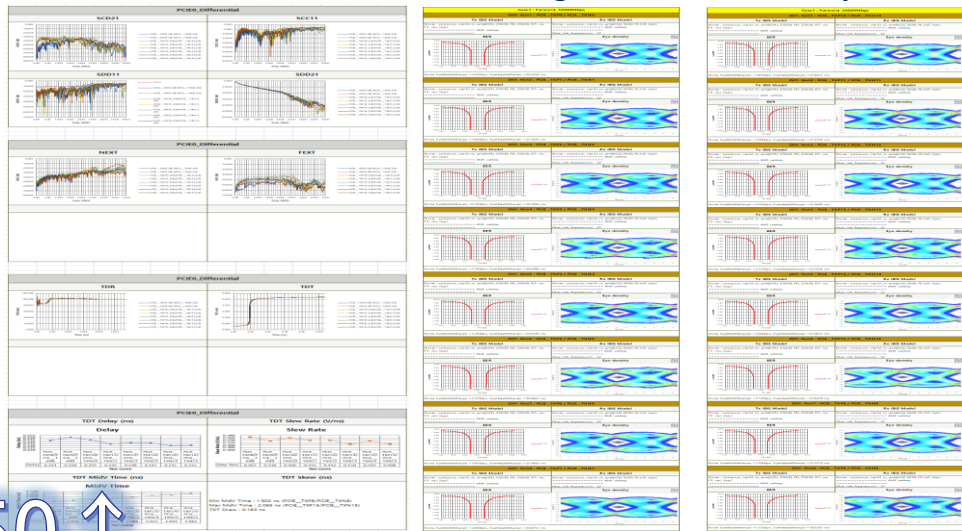
(Ignore_Bits (Usage Info) (Type Integer) (Default **2240000**))

Solution type	Conditions	Analysis time
Competitor-2	-manual setting (over ~1h) -without reporting	10h 20m / pair Total = 161h
Competitor-3	-Semi-automated configuration	15h / pair Total = 240h
ACVS	-auto setting -auto reporting	3 h 40 m

x50 ↑



Solution: ANSYS Ch. modeling + ACVS SI/PI analysis



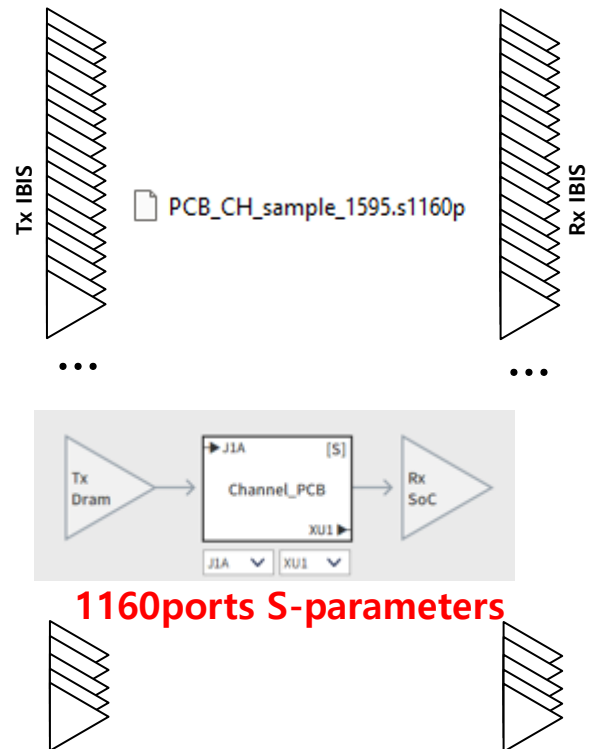
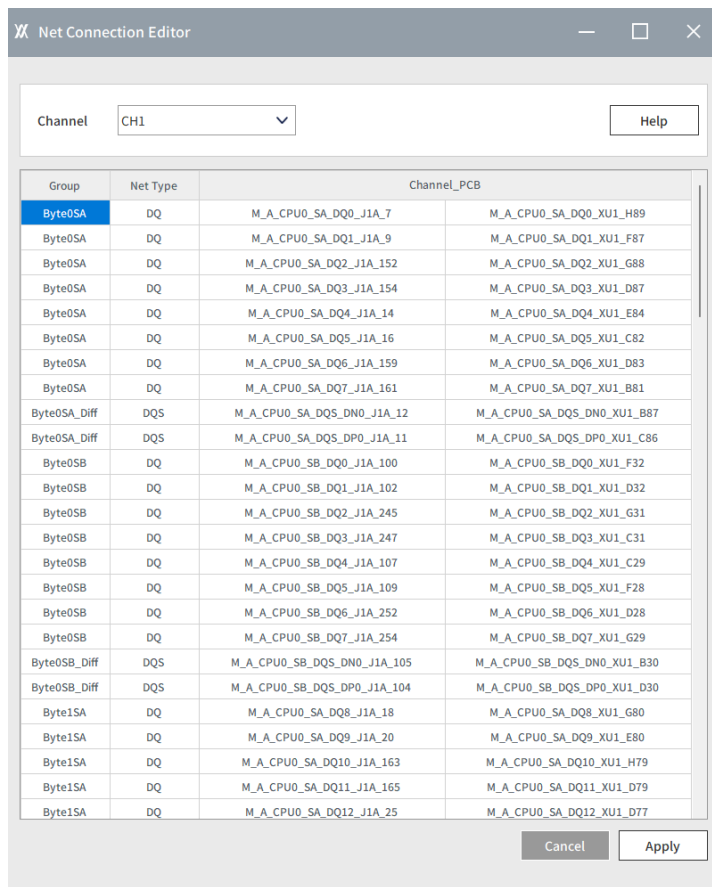
Basic-SI: 38m

AMI: 3h 40m

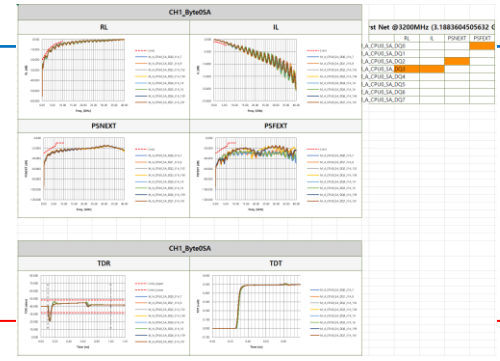
7. Memory module: Performance Highlights #1

Cases study: LPDDR5x (Transient simulation) 1160-ports Ch. model

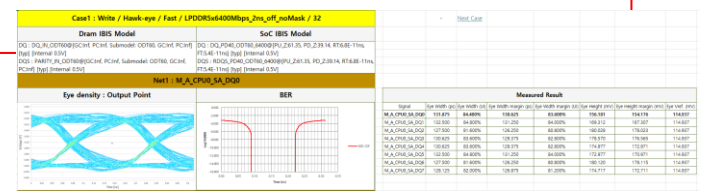
- ✓ 6.4Gbps, step->UI/32, sim. Hawk-eye Fast option setting
- ✓ Tx/Rx IBIS models: Non-linear model (Rising/falling waveform, pull-up/pull-down I/V data)
- ✓ Simulation environment: AMD Ryzen 32-Cores, 512GB RAM



LPDDR5x CH1/2/3/4 (s1160p)
(File Size : 111.5GB)



- Logs
- (BasicSI) 20250302093523_ACVS_Eval_v2025.1.2.2.PCPro.Beta.xlsx
 - (Memory-IBIS) 20250302093523_ACVS_Eval_v2025.1.2.2.PCPro.Beta.xlsx
 - (Memory-IBIS) 20250302093523_ACVS_Eval_v2025.1.2.2.PCPro.Beta_Full.xlsx
 - ACVS_Results_20250302093523.hcnx
 - Profile_ACVS_Results_20250302093523.ini



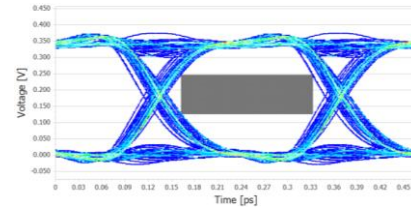
Solution type	Conditions	Analysis time
Competitors	Can not handle the large Ch. model	NA
ACVS	-auto setting -auto reporting	Basic SI: 6h Memory IBIS: 2h. 2m.

Transient simulation comparison

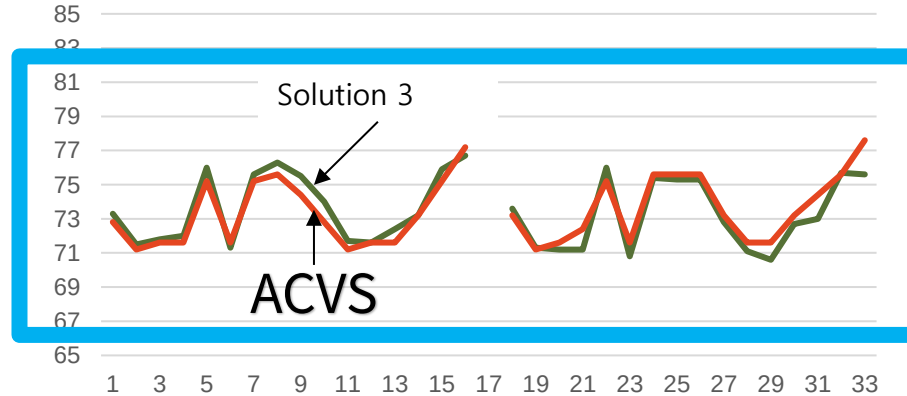
Cases study: User specific manual bit patterns (Transient simulation)

- ACVS < 6 min
- Competitor < 6 hour

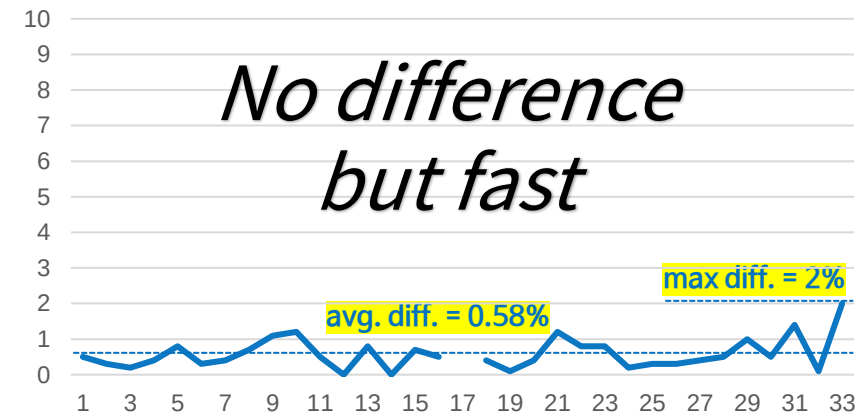
x60 ↑



Eye width (% , UI)



Error (% , UI)



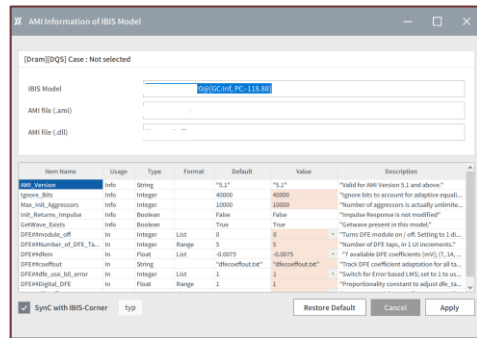
*No difference
but fast*

* The predetermined bit pattern had been applied.

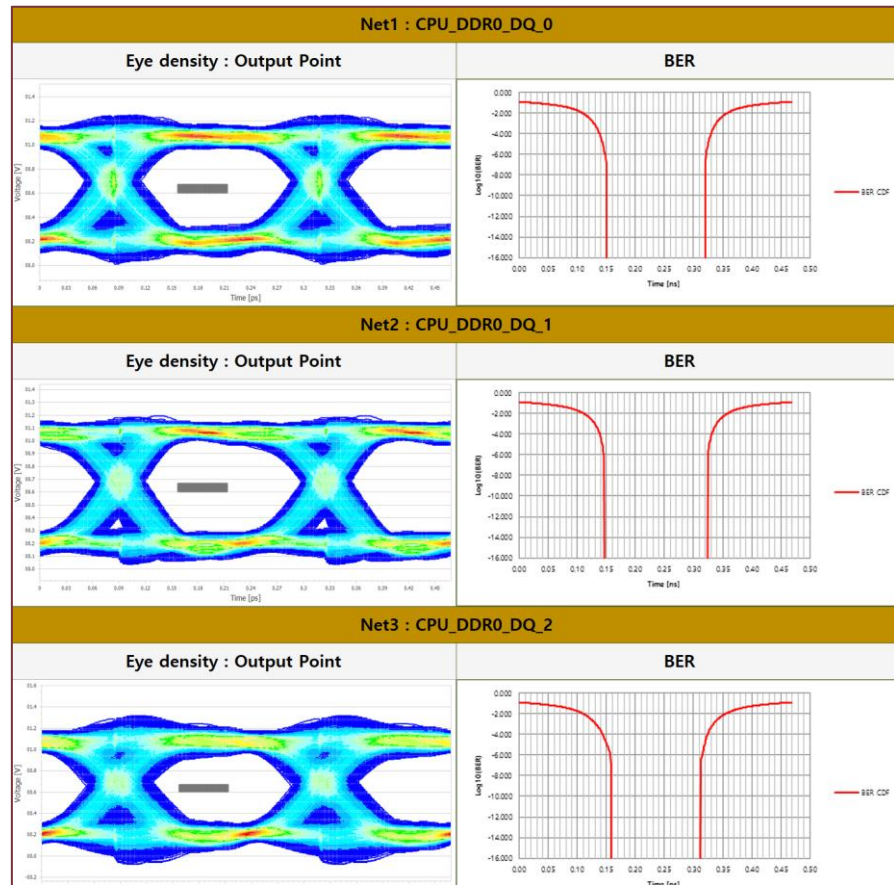
- Precise impulse responses (**w. full X-talk**): Higher accuracy
- The dedicated memory AMI solver structure: Higher speed
(Automation for processing multi-edge responses, DC offset, Forward clocking)



Accuracy/Time
guaranteed



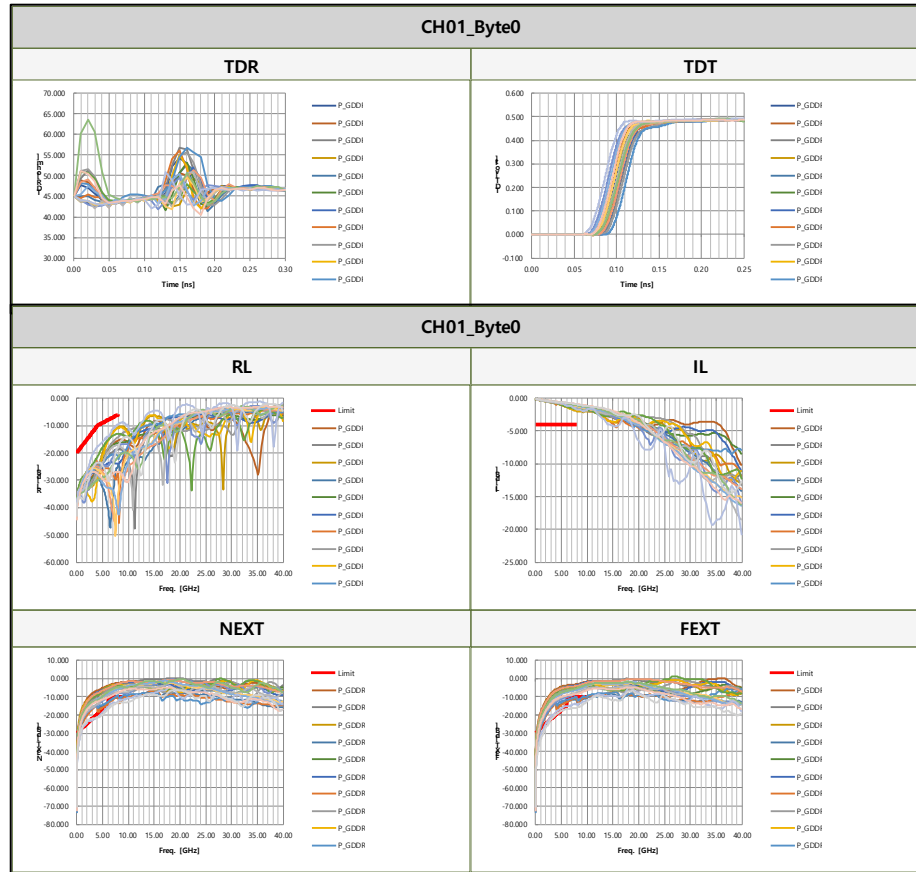
Signe-ended AMI option
for DDR5, GDDR6 analysis



Support Memory AMI

Case study: AI Chip Ch. Verification Example

- AI Chip Complexity : PCIe Gen5(32Gbps x 32ch.), GDDR6(16Gbps, > 300 I/O nets), HBM3(6.4Gbps, 1024 I/O nets)
- Full Ch. X-talk sum, TDR, BER/Eye Verification needed
- Schematic base manual verification is difficult (time and human error issues)



Basic-SI: 2h. 40m (GDDR6 8 Bytes)

Total analysis time < 10 hour

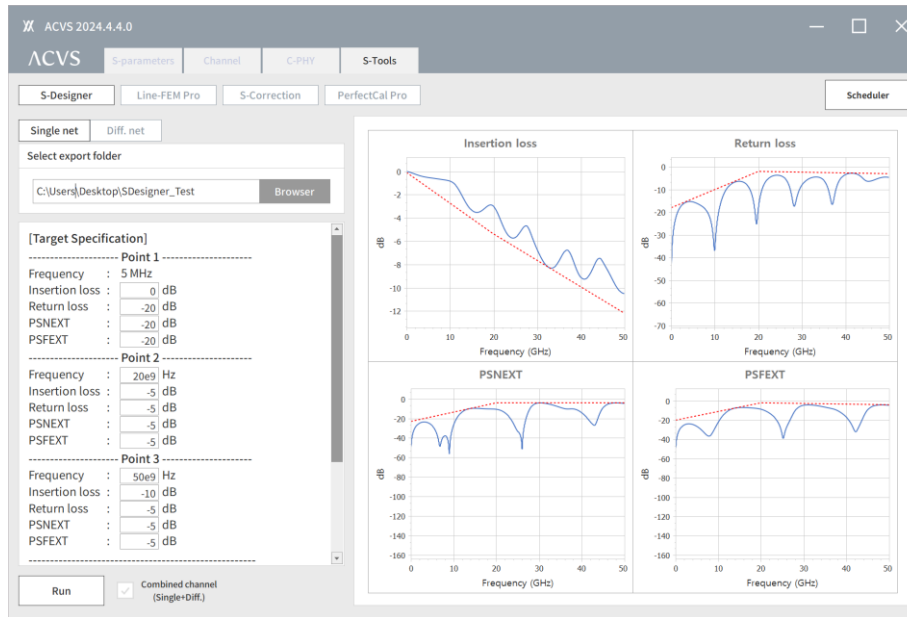


AMI analysis: 6h.30m (GDDR6 8 Bytes)

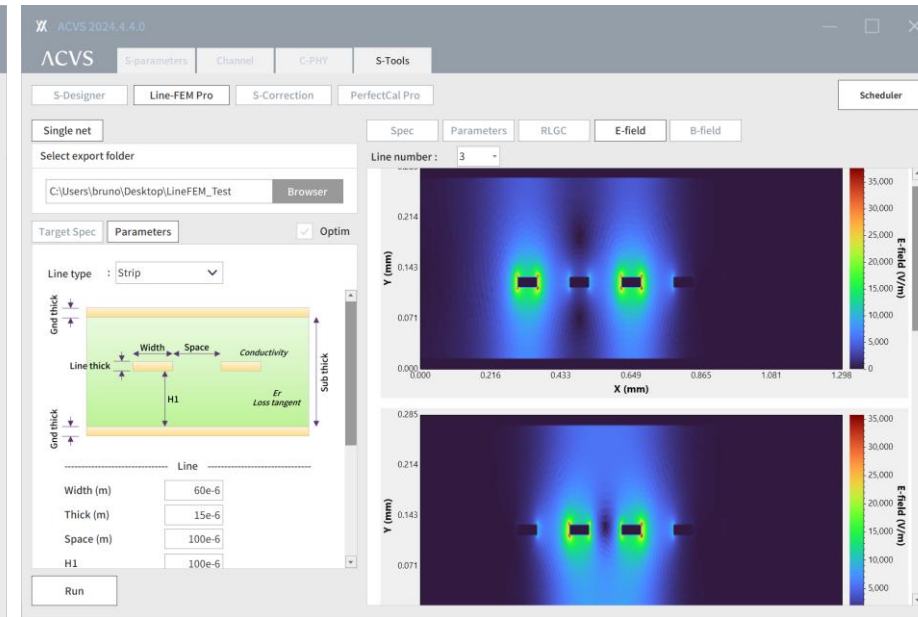
S-Designer: Rapid S-parameters generation for the given IL/RL/X-talk conditions.

Line-FEM Pro: High-precision transmission line design tool utilizing 2D FEM.

(Exports S-parameters, W-elements files)



S-Designer



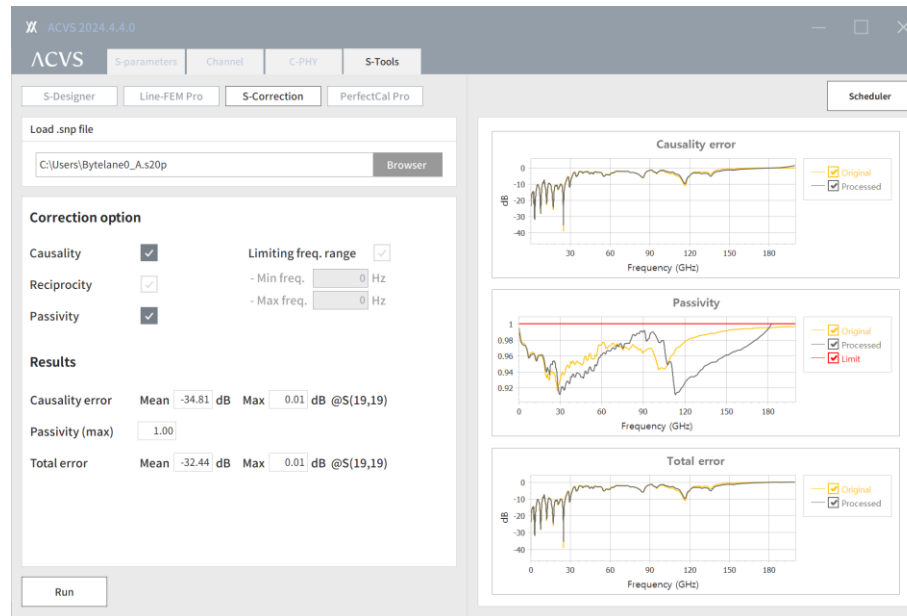
Line-FEM Pro

S-Correction: Resolves causality and passivity issues in S-parameters.

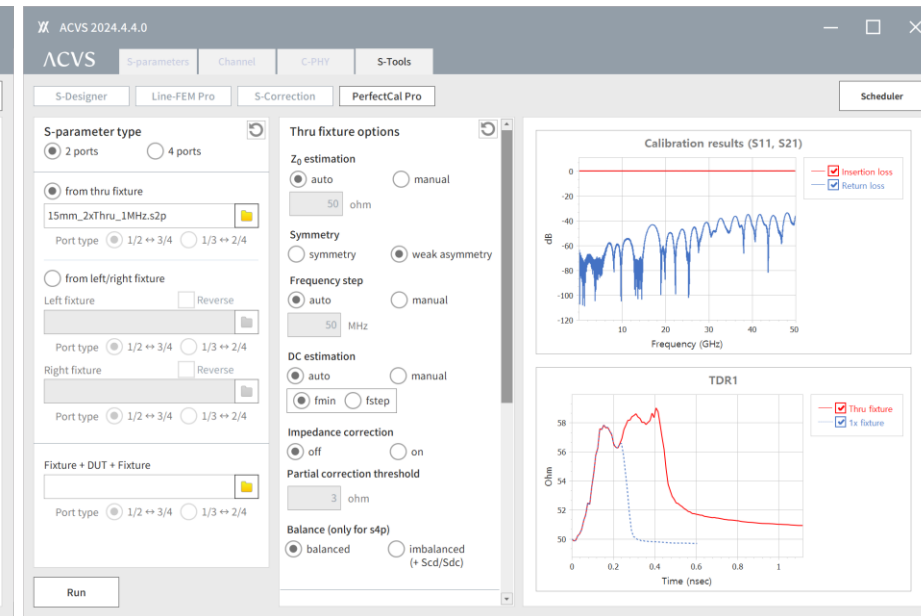
(Enforcement of causality, reciprocity, and passivity of given S-parameters)

PerfectCal Pro: Professional-grade 2xThru fixture de-embedding solution.

(Supports asymmetry, impedance correction; IEEE P370)



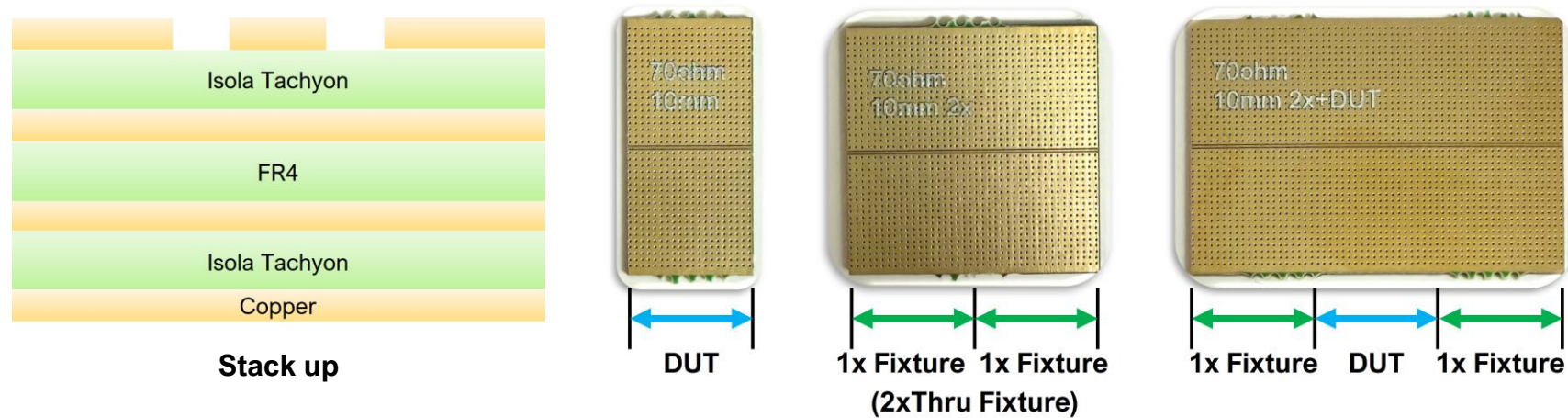
S-Correction



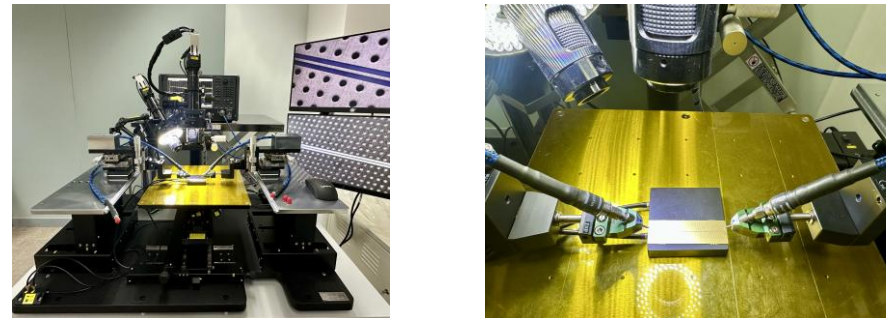
PerfectCal Pro

Cases study: De-embedding up to 50GHz

- Design: CPWG based 2xThru, 1x Fixture, DUT
- Measurement: Keysight PNA N5225B, T-plus uProbe



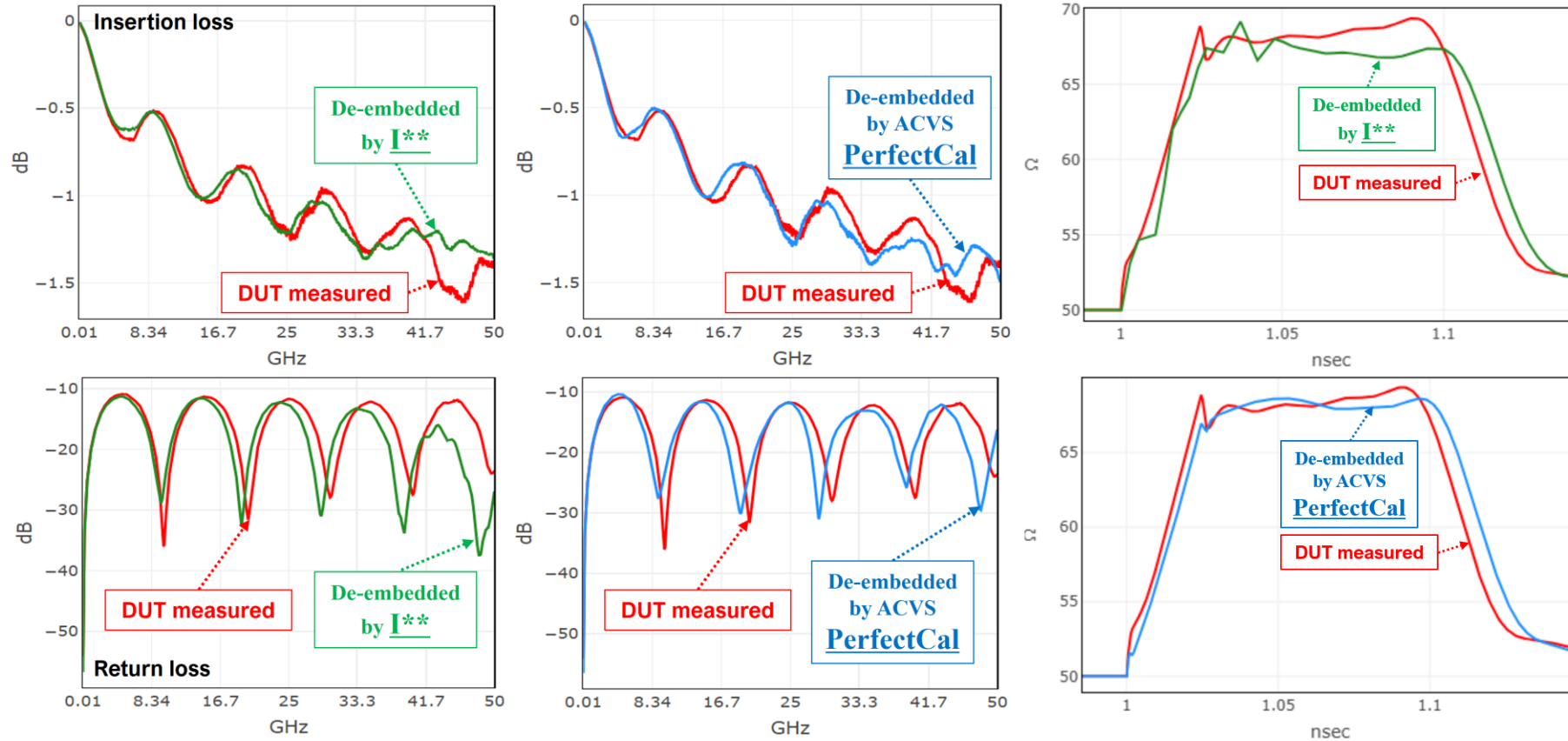
DUT: CPWG 10mm (Z_0 : 70 ohm) and 2xThru Fixture



Measurement Setup @ Huwin Lab
(Keysight PNA N5225B, T-plus uProbe)

Cases study: De-embedding up to 50GHz

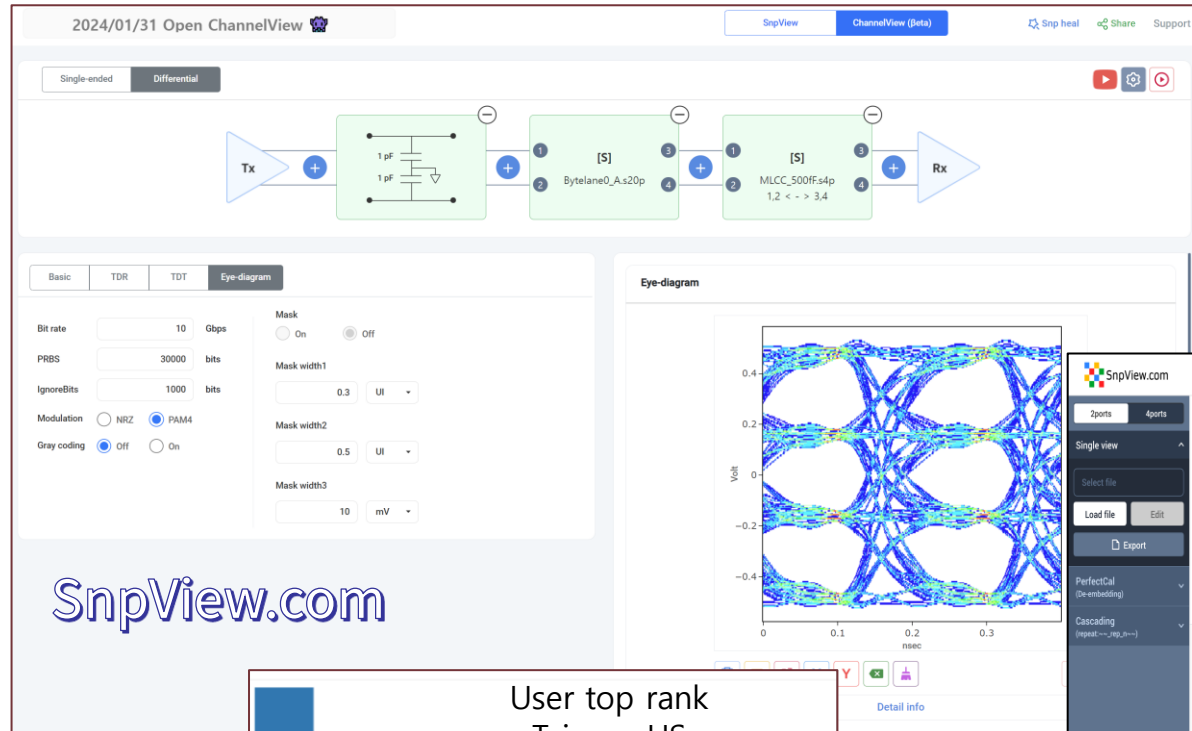
- Design: CPWG based 2xThru, 1x Fixture, DUT
- Measurement: Keysight PNA N5225B, T-plus uProbe



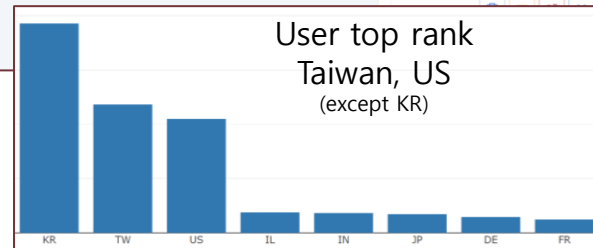
Direct Probing(DUT measured) vs De-embedded(I** vs ACVS PerfectCal Pro)

A High-Value, Professional Signal Integrity Simulator—Free to Use Online

- Basic charts: dB/phase, real/img, smith chart, group delay, passivity
- Advanced charts: **TDR, TDT, Eye-diagram (w. EQ, Jitter, Noise)**
- Advanced functions: **PerfectCal®** (lite), Snp Heal
- Powered by **SimNX**

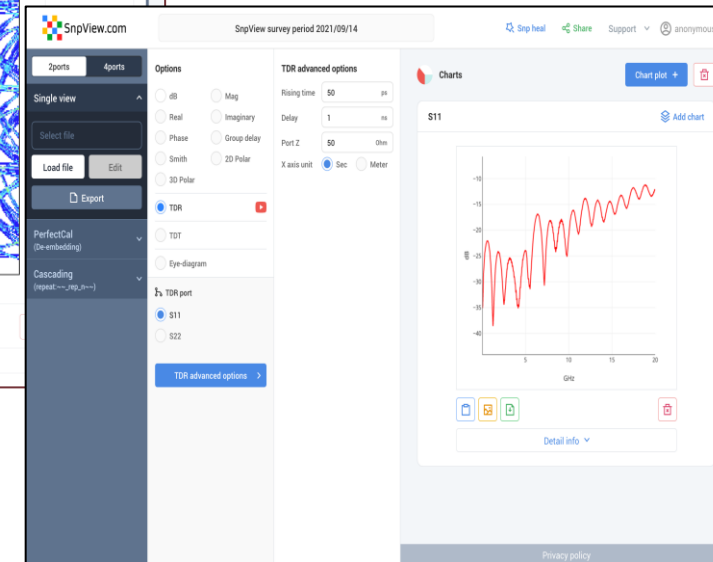


SnpView.com



Visitors
✓ 500~1000/day

Powered by SimNX



- 1) ANSYS EM(HFSS, SIwave), Cadence EM(Clarity, PowerSI) users.
- 2) HBM3(up to 12Gbps), DDR5(up to 6.4Gbps), LPDDR5(up to 9.6Gbps), GDDR6(up to 20+Gbps)
or faster memory PKG/PCB designer
- 3) PCIe gen5(32Gbps), PCIe gen6(64Gbps) PKG/PCB designer
- 4) AI chiplet Serdes interface (PCIe/CXL - C2C Interface, UCIe - D2D Interface, NVlink - Nvidia Interface ...)
-> PKG/RDL/Silicon interposer designer
- 5) AI chiplet memory DRAM interface (GDDR6, HBM3, LPDDR4 ...)
-> PKG/RDL/Silicon interposer designer
- 6) Who is struggling with the time domain (Eye/BER, TDR/TDT, Jitter) analysis fail problems
using the large size S-parameters (large port numbers/ high frequency bandwidth).
- 7) Who is struggling with channel configuration, verification and report generation
(talke long times for design revision issues) using the large size S-parameters
(large port numbers/ high frequency bandwidth).
- 8) Who is struggling with lacking the expertise/experience for the channel verification
and need the consultation service for EM model extraction and verification.
=> Huwin can support the ACVS users by extra consulting service, customer training/supporting.